

Potential for a smart sensor based on an integrated silicon anemometer

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Abstract

An intelligent silicon anemometer is being developed with a bridge which employs diffused resistors operated at an elevated temperature to achieve a high dynamic range. A novel technique achieves thermal feedback in a double Wheatstone bridge configuration using integrated temperature-insensitive operational amplifiers. The aim is to achieve high sensitivity, immunity from humidity and from ambient temperature variations. Early devices have been fabricated in CMOS technology demonstrating the efficient implementation of high performance analogue electronics suitable for using low-cost standard IC fabrication processes. An application for this integrated smart silicon anemometer is to replace the more cumbersome mechanical peak-flow meters used in the treatment of sufferers of chronic obstructive pulmonary diseases [1]. The reliability and immunity from interference can be further improved by integrating the complete sensor system on a single monolithic CMOS or BiCMOS chip.

Keywords: Smart sensor; Silicon anemometer; Wheatstone bridge

1. Introduction

Thermal flow sensors were introduced in the last century in the form of simple constant current anemometers. Today the constant temperature hot wire anemometer (HWA) is capable of sensing high frequency flow variations such as turbulence [2]. For spot measurements hot-wire anemometry is outperformed by laser doppler anemometry, but at a considerable price premium. As well as their use in anemometry, thermal flow sensors find applications in fluid and gas flow systems for both point velocity and volumetric flow measurement.

In the last decade, commercial silicon planar processing has gone through rapid market-driven evolution from pure bipolar technologies to high performance CMOS and BiCMOS. Now we see microengineering techniques being used for example, in smart sensors developed for the automotive and aerospace industries. These trends have led to the development of intelligent flow sensors on silicon for a variety of applications [3].

This paper presents an implementation of an integrated silicon anemometer using a 2.0 μm commercial CMOS process with no additional processing steps.

Two-stage Miller compensated CMOS operational amplifiers were integrated along with several device test structures in order to evaluate high temperature circuit performance. Thick-film technology was used to package the device for initial measurements, using an unconventional mounting technique discussed in Section 4.1.

1.1. Hot wire anemometry

Conventional HWAs usually operate on the Wheatstone bridge configuration. A tungsten wire mounted on the tip of a probe forms one of the bridge elements and a second, variable bridge element is used to set the operating point. In constant current mode shown in Fig. 1(a), the bridge supply current is maintained constant and a flow calibration curve is used to read a flow value for a given imbalance voltage under flow conditions. The frequency response is low because of the delay in establishing a potential difference across the bridge measurement nodes for a given signal change. The alternative, constant temperature mode, illustrated in Fig. 1(b) uses a feedback controller to maintain the sensor at a constant temperature (or at a constant temperature differential above ambient). Under flow, the controller increases the power supply to maintain a balanced bridge. The current required to achieve

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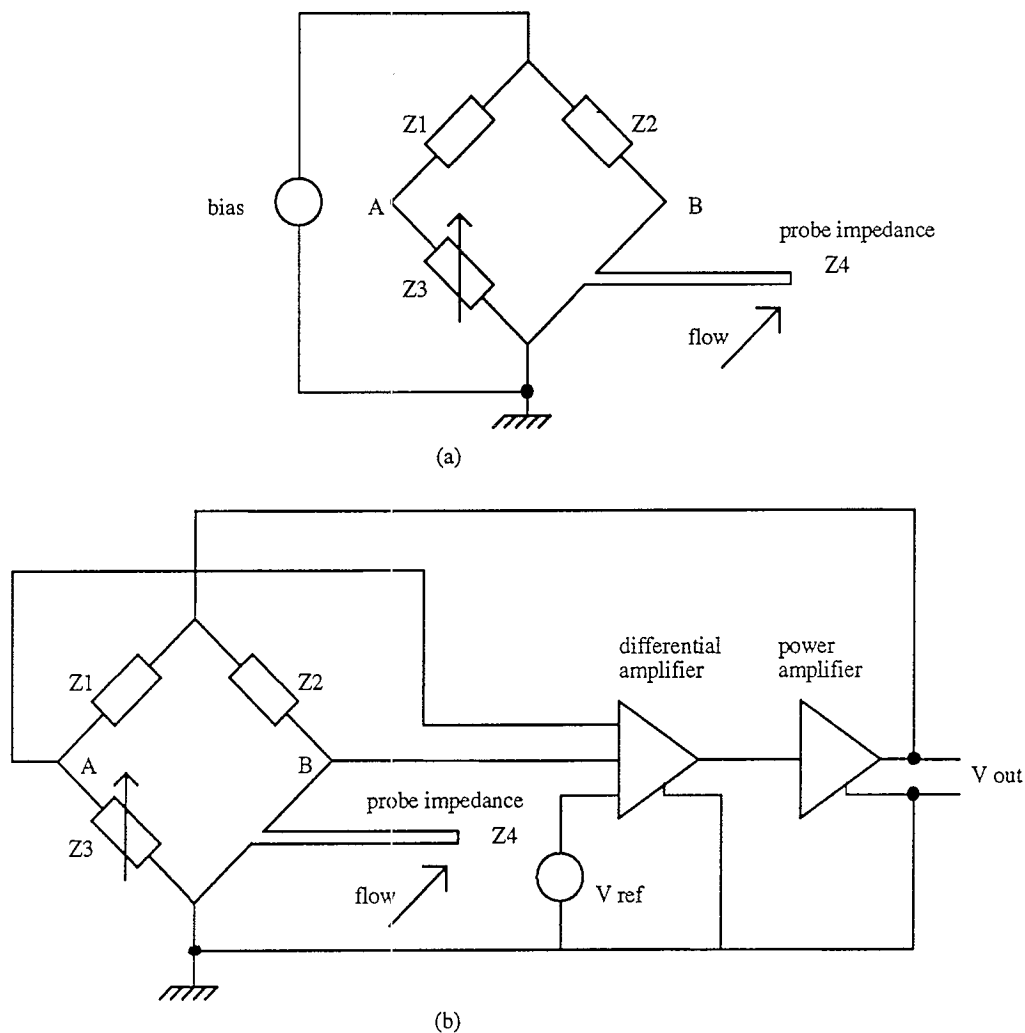


Fig. 1. Hot wire anemometer: (a) constant current mode; (b) constant temperature mode.

balance is a measure of the flow. This method allows high-frequency flow fluctuations to be measured since the electrical time constants are much shorter than thermal.

Several authors have demonstrated feasible integrated flow sensors using thermopiles [4], diodes [5], vibrating cantilevers and microbridges [6,7], diffused [8] and polysilicon resistors [9]. Microengineering techniques have been used to reduce thermal mass [10], to provide thermal isolation [5] and a repeatable flow characteristic [11].

2. Integrated Wheatstone bridge anemometer

The integrated Wheatstone bridge shown in Fig. 2(a) is a monolithic implementation of hot wire anemometry [12]. Constant temperature mode is achieved through the use of a comparator or summing amplifier which compares the temperature dependent feedback from the measurement bridge fed with a constant voltage or current, with a reference voltage. The resulting error signal is power amplified and used to drive the heater bridge which is thermally connected to the measurement

bridge. The result is constant average measurement bridge resistance with flow. The advantage of this configuration is that the frequency response can be high. Dynamic range is also improved since two sensor elements are being excited by the flow. A disadvantage is that a larger proportion of the heater current flows in the coolest side, so the heater in this case tends to reduce the thermal gradient which is generating the signal. This is negative feedback.

Alternatively the double bridge configuration can also be used in constant heater current mode. In this way the heater current is fixed for varying flow conditions. The advantage is that the signal level obtainable is high although the signal is now a function of the power supply. The principle is demonstrated in Fig. 2(b).

2.1. Sensing elements

The number of bridge elements which are active determines the maximum signal level possible. For a 2D sensor one or two sensors can be used. It can be shown that for maximum sensitivity in the Wheatstone Bridge

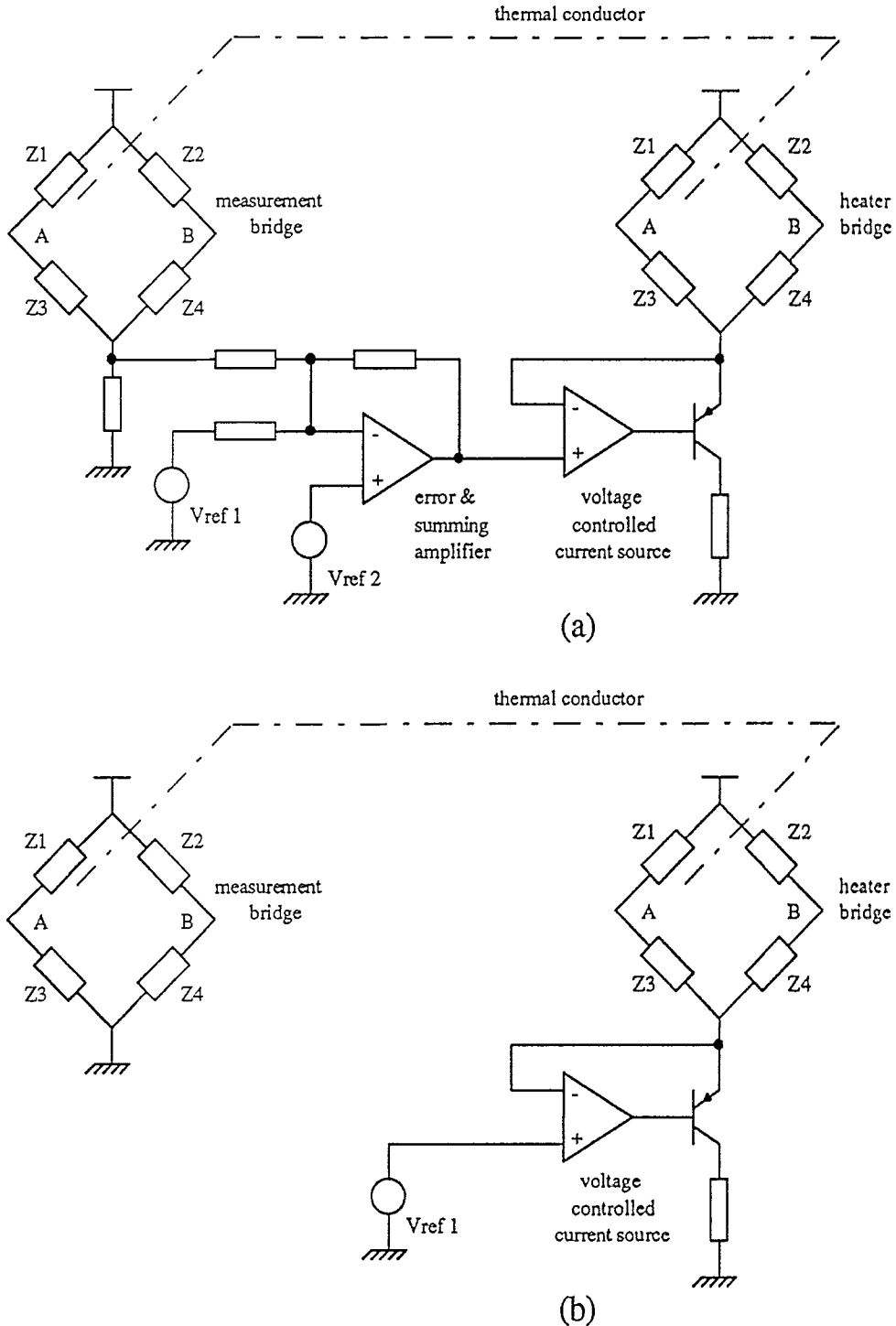


Fig. 2. Integrated Wheatstone bridge: (a) constant temperature mode; (b) constant heater current mode.

$$Z_1 = Z_3 \text{ and } Z_2 = Z_4 \tag{1}$$

If the change in a bridge element resistance caused by the flow is denoted by δZ , then we find that for the deflection method

$$V_{AB} = V_I \frac{Z(1+\delta)}{Z(2+\delta)} - \frac{Z}{Z(2+\delta)} \tag{2}$$

where Z is the bridge impedance.

This can be simplified to

$$V_{AB} = V_I \frac{\delta}{2+\delta} = V_I \frac{\delta}{2} \tag{3}$$

The highest signal amplitude is obtainable by having all four elements as sensors or signal sources. This is twice the signal amplitude available if only one element is used for measurement. It is important to ensure matching to avoid offset. An advantage of using two

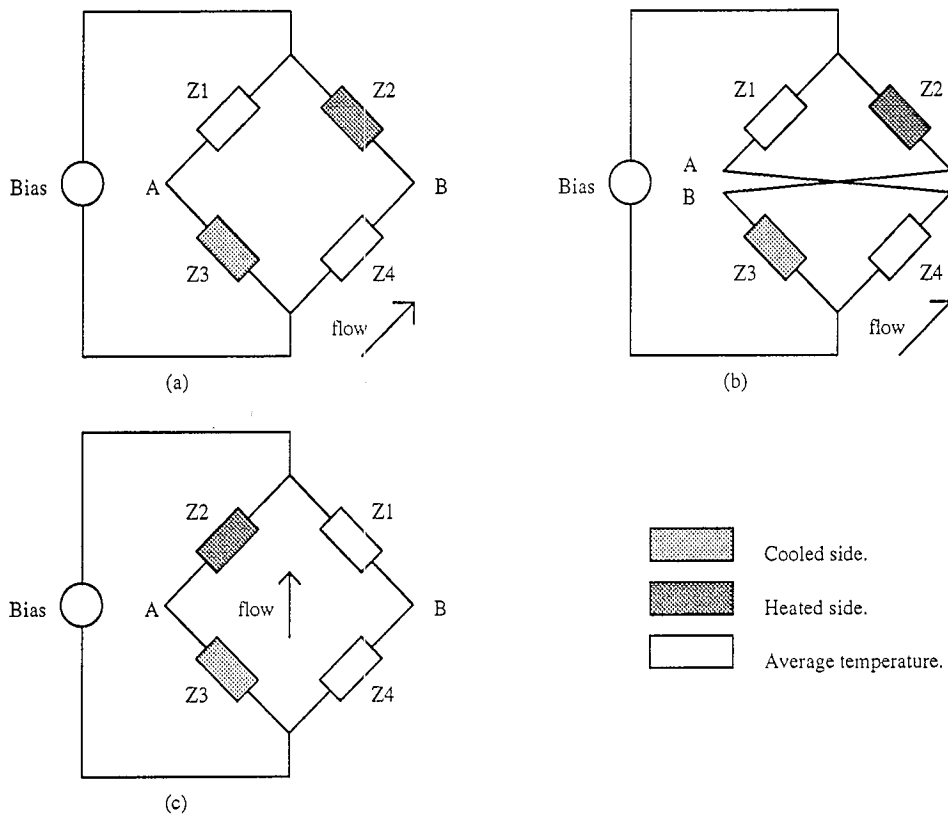


Fig. 3. Improving the signal level using alternative sensor positions within the bridge.

measuring elements is that a bipolar signal is available.

The way in which the sense elements are interconnected also has a significant effect on performance. Consider the measurement bridge shown in Fig. 3(a). Assuming that all resistance values are equal and have a high positive temperature coefficient, when flow crosses Z_3 and Z_2 , Z_3 is cooled and Z_2 is heated with respect to average sensor temperature. The result is that V_A and V_B both decrease. However because of the fact that the heating of Z_2 is less than the cooling of Z_3 we obtain a potential difference V_{AB} . By slight modification to the chip metallisation it is possible to improve greatly the level of signal generated. If nodes A and B are split and then cross-coupled as shown in Fig. 3(b), then the two sensing elements are effectively on the same side of the bridge, Fig. 3(c). Now the signal is the 'sum' of δZ_2 and δZ_3 and not their difference.

3. Intelligent flow sensors

There are numerous advantages to integrating the readout and signal processing electronics with sensors [13]. The usual requirements are current or voltage amplification, filtering and linearisation. The operational amplifier is the basic building block for all of these functions. Circuits which are tolerant of elevated temperatures would find a use with intelligent thermal flow sensors. One of the most effective methods of reducing

temperature drift in CMOS operational amplifiers is to bias the gain stages at their zero temperature coefficient (ZTC) bias points. Biasing the current sources for each stage at their respective ZTC gate source voltage in the saturation region is a simple way of achieving this [14]. Fig. 4 contains measurement results for a PMOS device which we fabricated in order to test the ZTC bias principle.

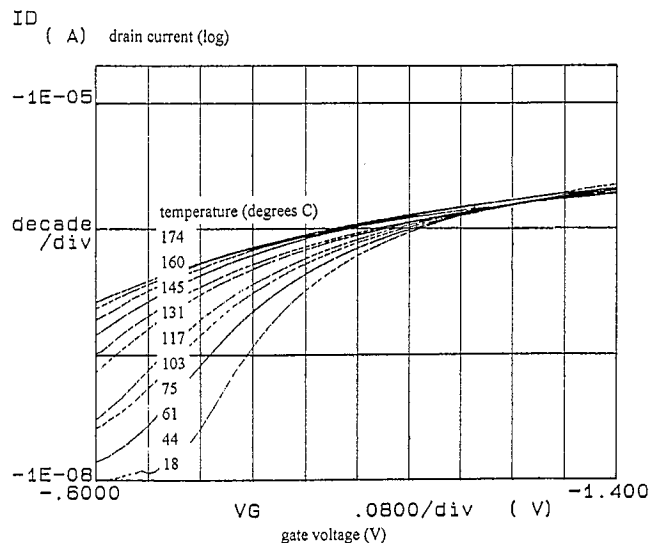


Fig. 4. Zero temperature coefficient (ZTC) bias point for CMOS operational amplifiers.

4. Design and fabrication

We have fabricated two different sensor designs with the connection patterns shown in Fig. 3(a) and (b). For Fig. 3(a) the two sensing elements are on opposite diagonals of the bridge. In Fig. 3(b) the sensors are both effectively on the same side of the bridge. An inner bridge makes up the heater and uses resistors with aspect ratios identical to those in the measurement bridge. The sensor elements are n-well diffused resistors with a sheet resistance of 2000 Ω per square and a value of 41 Ω . The temperature coefficient of the material is given in the equation

$$R_T \cong R_0(1 + \alpha(T_1 - T_0)) \quad (4)$$

where R_0 is the resistance at a reference temperature T_0 , R_T is the resistance at an elevated temperature T_1 and α is the temperature coefficient of the material.

Extra wide metallisation has been used to avoid exceeding the maximum allowable current density for this layer. The central area (core) of the chips has been used to fabricate some test structures which may be used in the final smart sensor design. These include operational amplifiers with and without a bias chain, different bias circuits, active and passive components for temperature coefficient extraction and an automatic ZTC bias generator cell. Because of the unconventional use of the chip periphery to fabricate a sensor, a second pad ring has been laid out between the sensor and the core circuitry in both cases.

4.1. Hybrid packaging

A 14-pin, dual in line (DIL) ceramic chip carrier has been used to mount the sensors so that they are accessible to the air flow. Although the alumina material in the substrate is a good heat conductor the die has been raised 50–100 μm above the surface using a printed thick-film dielectric material combined with a thermally non-conductive epoxy at each corner. For a die size of 10 mm^2 there is less than 1 mm^2 area in thermal contact. Printed gold tracks have been used to facilitate thermosonic wire-bonding of the die to the hybrid shown in Fig. 5. For flow testing the hybrids have been mounted on a printed circuit board at the end of a stainless steel tube.

5. Experimental results

The resistance value for both heater and sensor was measured to be 41.6 Ω at 23 $^\circ\text{C}$. Fig. 6 shows a plot of measured resistance versus temperature for the device. The high sheet resistance of the well resistors yields the high positive temperature coefficient required to give a large signal for small bridge imbalances. The

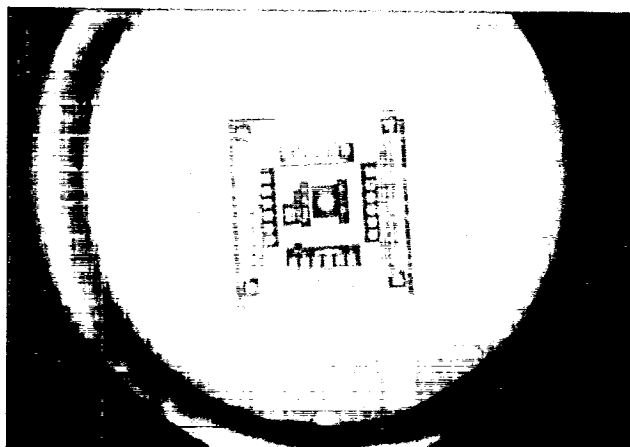


Fig. 5. Hybrid packaging.

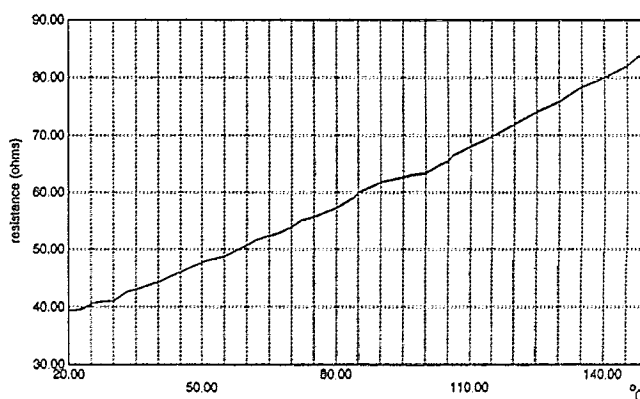


Fig. 6. Measured bridge resistance vs. temperature.

equivalent resistance of the bridge is approximately doubled at 140 $^\circ\text{C}$.

The air flow tests were done at room temperature using a wind tunnel with a calibrated hot film anemometer mounted the same distance into the test chamber as the sensor under test. For both sensor structures measurements were carried out using both constant temperature and constant heater current modes. The proportional gain for the constant temperature controller was set to 150 000 which reduced the transient response time for the heater from 300 to 3 ms with no overshoot. Above that gain level the controller became unstable. Figs. 7 and 8 illustrate the variation in heater current with flow and the constant sensor bridge current respectively.

A fully differential current-to-voltage converter was used to maintain the measurement bridge in the nulling configuration whilst allowing a better common mode rejection ratio. Fig. 9 shows the differential output voltage from the current-to-voltage converter for chip 1 for 3–15 m s^{-1} air-flow. The gain factor used was 560 V A^{-1} . A zero flow offset voltage of approximately 2 mV was measured for the both sensors. The results given have been adjusted for offset. Measurements were taken for constant temperature mode and for two values of constant heater current. It was found that using

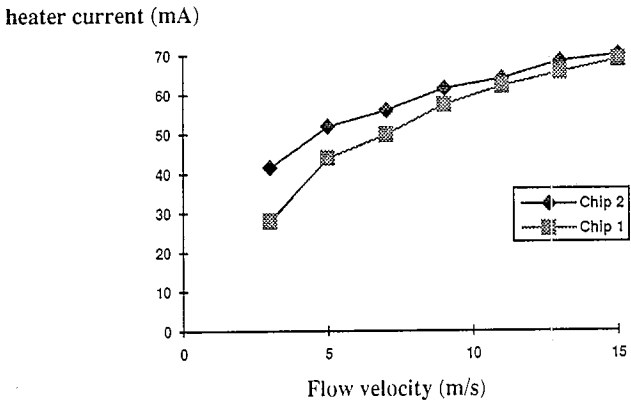


Fig. 7. Heater bridge current as a function of flow velocity (constant temperature mode).

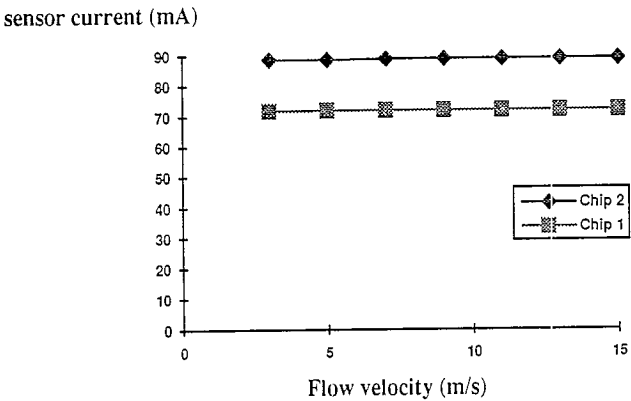


Fig. 8. Sensor bridge current as a function of flow velocity (constant temperature mode).

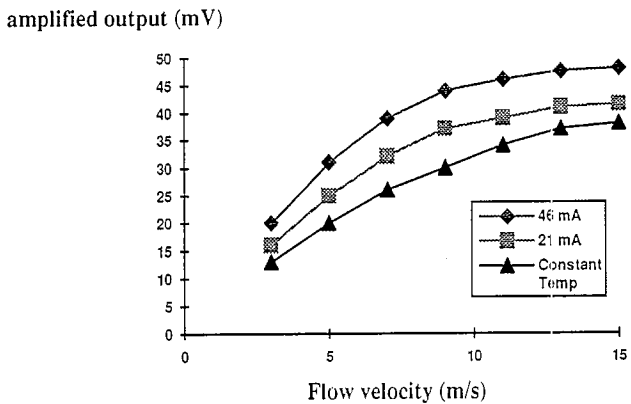


Fig. 9. Chip 1 output voltage as a function of flow velocity with heater current as a parameter and for constant temperature mode.

constant temperature the maximum signal range is lower than for a constant heater current. The plots confirm that a higher sensor temperature yields a higher signal level in constant current mode. It is also clear that in constant temperature mode the signal is being reduced by negative feedback. For chip 2 (Fig. 10) a similar set of results was obtained. However there is a tenfold increase in output signal when the layout in Fig. 3(c) is used. At lower flow rates it appears that there is a

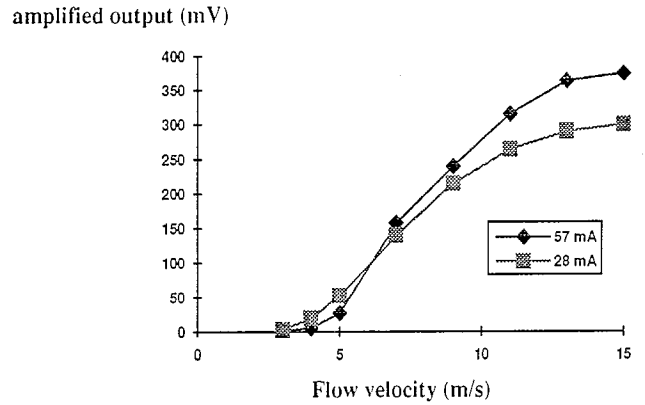


Fig. 10. Chip 2 output voltage as a function of flow velocity with heater current as a parameter.

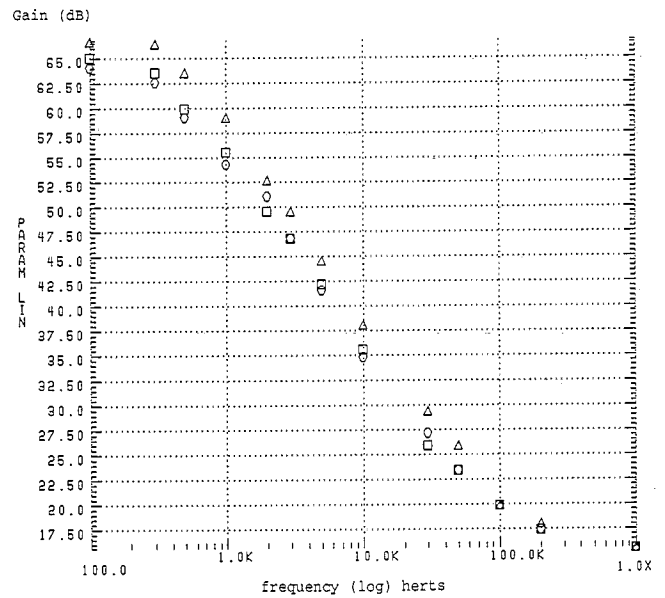


Fig. 11. Gain (dB) vs. frequency with temperature as a parameter: (Δ) 40 °C; (\square) 100 °C; (\circ) 140 °C.

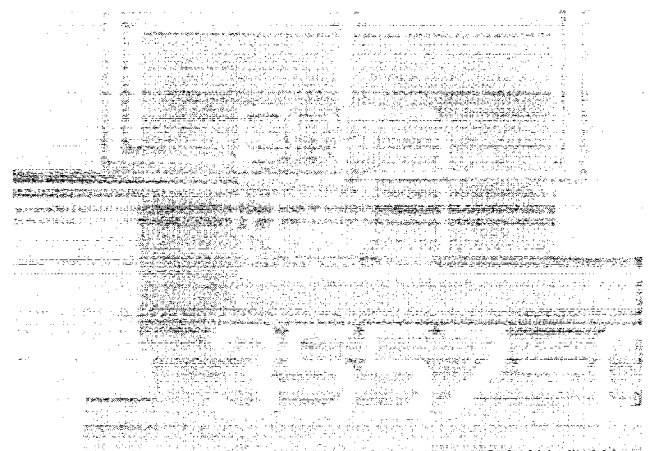


Fig. 12. Photomicrograph of operational amplifier and bias chain.

threshold flow rate below which the sensitivity of this configuration is reduced. Clearly from the results shown in Figs. 7 and 8 the power dissipation is high. However

the device has been fabricated using an unmodified mixed-mode CMOS process. If power dissipation can be traded off against cost then the performance-to-price ratio for this sensor is good.

The integrated operational amplifiers were tested using the integrated Wheatstone bridge to heat the chip to various temperatures. Fig. 11 summarises the results for these full-custom analog cells. Clearly there is a small reduction in open loop gain at elevated temperatures. Fig. 12 shows a photomicrograph of a single Miller compensated op-amp cell. The op-amp layouts were optimised for minimum area.

6. Conclusions

The integrated Wheatstone bridge structures in chips 1 and 2 are both viable air flow sensors in a standard CMOS process. Constant temperature operation tends to lower the output signal level due to the uneven current distribution in the heater bridge under flow with this heater layout. A new heater layout located at the centre of the chip would appear to be more suitable. Chip 2 has a much higher signal amplitude since its output depends on the sum of two δZ values while chip 1 uses their difference. The power dissipation for both designs is high and needs to be reduced using wet or dry etching. This will also aid in increasing the frequency response. Finally it has been shown that it is possible to operate conventional operational amplifiers biased close to their ZTC gate source voltage at elevated temperatures with tolerable gain reduction.

7. Future work

At the time of writing we are fabricating a new sensor layout which uses all elements in the bridge as sensors, and utilises a split heater which allows current division to be controlled so that the signal is not reduced using the constant temperature mode of operation. We are also using deep plasma etching and wet maskless etching with EDP solutions to perform bulk and surface micromachining for thermal isolation and to reduce thermal mass. We also intend to investigate the use of polysilicon as the sensor material which will allow fully suspended Wheatstone bridges. Complete signal

processing systems will be tested using the temperature insensitive op-amps currently being tested.

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