Time Behavioral Model for Phase-Domain ADPLL based Frequency Synthesizer

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***Abstract* — In this paper, we present a Time Behavioral Model of a recently proposed Phase-Domain All-Digital Phase-Locked Loop (ADPLL) for RF applications. This model can be easily implemented, and results in a versatile and fast ADPLL simulator that enables to study many aspects of the PLL, e.g. transient responses, steady states, limit cycles, or to perform perturbation analysis. Moreover, we present a baseband analysis that allows to compute the power spectral density from the instantaneous frequency obtained as the output of the behavioral model. Simulations illustrate the effectiveness of this new behavioral model.**

***Index Terms* — Phase locked loops, modeling**

I. INTRODUCTION

Recently, a new All Digital Phase-Locked Loop based RF frequency synthesizer was presented by Staszeswski *et al.* [1]. A block diagram of the proposed architecture is shown in Fig 1.

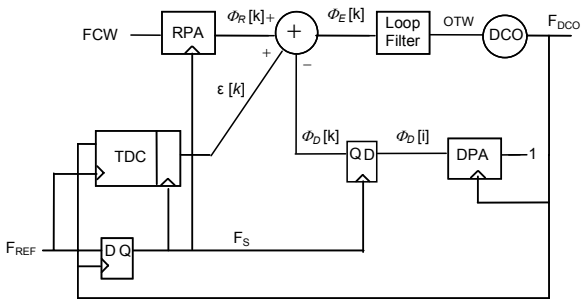

Fig 1. ADPLL based RF frequency synthesizer [1]

A digitally controlled oscillator (DCO) allows for this PLL to be implemented in a fully digital manner [2].

Phase accumulators are used to count cycle periods of reference and feedback oscillators. A synchronous clock, F_S, undersamples the output of the DCO phase accumulator (DPA), so that comparison of the two phases can be performed using the same clock. The retimed clock, F_S, is achieved by oversampling the reference clock, F_{REF}, by the oscillator clock, F_{DCO}.

Note that in Fig 1, index *i* and *k* do not refer to the same clock.

Higher ADPLL precision is obtained using fractionnal phase error correction. One can show that this fractionnal phase error is proportionnal to a time delay. The Time to Digital Converter (TDC) is used to convert the delay (phase) between the RF and reference clocks directly into a digital quantity [3], with a time resolution, noted ΔT_{RES}, that can be equal to the elementary propagation delay through an inverter gate.

The Frequency Command Word (FCW) is given as input to the reference phase accumulator (RPA), and enables to tune the output frequency of the DCO.

$$F_{DCO} = FCW \times F_{REF} \qquad (1)$$

Designing a PLL requires a simulator in order to study the effect of varying parameters and optimize the PLL.

Analysis and simulation of the ADPLL in Fig. 1, with a direct method requires a very high rate clock. Indeed, such a clock must have a rate that is greater than the highest frequency in the system. This requirement leads to an incredible simulation time and fantastic amounts of data.

The objective of this paper is to show that it is possible to simulate such a PLL at much more reasonnable rate, without sacrifying accuracy. The limiting components are the DCO phase accumulator (at F_{DCO} rate), and the TDC (with accuracy ΔT_{RES}), because of they would need an extremely fast sampling frequency for a correct representation. The key for developing new simulation model is to express behavior of limiting components outputs directly at rate F_{REF} but independently of internal rate F_{DCO} or time accuracy ΔT_{RES}. This can be understood as a kind of carrier frequency suppression.

In section II we consider the analysis of the simplest phase comparator: a D flip-flop, and so doing we present the basics of our behavioral model. Then, in section III we

develop the closed loop model; expressions of TDC and resampled oscillator phase accumulator outputs are derived using the analysis of section II. Next, we show how to derive the Power Spectral Density (PSD) from the instantaneous frequency obtained at the output of the DCO. Finally, we show typical results obtained using the behavioral model and we make simulation comparison with a conventional VHDL model.

II. Principle of Behavioral Model

In order to understand the principle of the behavioral model, we focus on simple D flip-flop. Indeed, this central element links asynchronous clocks F_{DCO} and F_{REF} because it resynchronizes them.

Let us consider the waveform shown in Fig 2. In this diagram two important parameters appear: the delay τ_k and the integer value *N(k)*. τ_k is defined as the difference between the k^{th} reference rising edge and following oscillator rising edge, and *N(k)* is the real-value count of the DCO clock periods $T_{D,k}$ for each cycle of the reference clock.

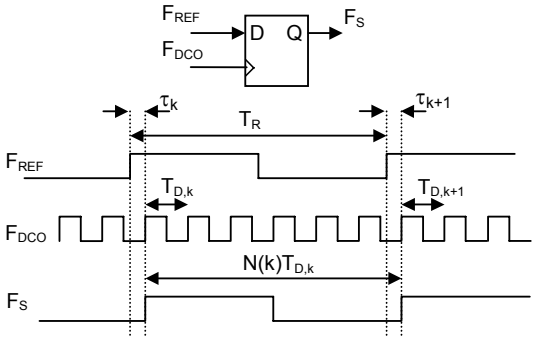

Fig 2. Inputs/output of the D flip-flop with a representative set of waveforms

The exact relation between reference and oscillator frequencies can be deduced from the waveform in Fig 2. We obtain the following relashionship between τ_{k+1} and τ_k

$$\tau_{k+1} = \tau_k + N(k)T_{D,k} - T_R \qquad (2)$$

where T_R is the period of the reference clock and $T_{D,k}$ is the DCO period during the k^{th} F_{REF} cycle. An important point is that the time delay is bounded according to

$$0 \le \tau_{k+1} \le T_{D,k} \qquad \forall k \qquad (3)$$

Another essential remark is that the phase error in the PLL is directly proportionnal to this delay.

Equation (2) is valid if $T_{D,k}$ remains constant during a whole cycle of F_{REF}. Let us define by $N_i(k)$ the integer part of the ratio between the two periods defined above

$$N_i(k) = \lfloor T_R / T_{D,k} \rfloor \qquad (4)$$

In (2) we have either $N(k) = N_i(k)$ or $N(k) = N_i(k) + 1$. Hence the behavior of the D flip-flop is equivalent to a Dual Modulus Divider (DMD) controlled by the phase error (via the delay τ) as shown in Fig 3. In an extented model taking into account possible variations of $T_{D,k}$ during F_{REF} cycle, we may represent *N(k)* by *N(k) = Ni(k) + C(k)* where *C(k)* is a natural number.

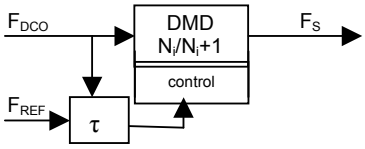

Fig 3. Behavioral model of the D flip-flop by a DMD controlled by the phase error

In the case where *N(k)* take only two values, computation of *N(k)* proceeds as follows.

First suppose that $N(k)=N_i(k)+1$, and compute τ_{k+1} using (2). Then, we have to check that (3) is satisfied. If it is, we keep $N(k)=N_i(k)+1$, otherwise $N(k) = N_i(k)$.

This analysis results in the following equations:

$$\tau(k+1) = \begin{cases} (N_i+1)T_{D,k} - T_R + \tau(k) & \text{if} \quad \tau(k+1) - T_{D,k} < 0 \\ N_i T_{D,k} - T_R + \tau(k) & \text{otherwise} \end{cases} \qquad (5)$$

This can be further simplified into

$$\begin{aligned} \tau(k+1) = \tau(k) &+ \left(N_i(k) + 0{,}5\right)T_{D,k} - T_R \\ &- \operatorname{sgn}\left(N_i(k)T_{D,k} - T_R + \tau(k)\right)T_{D,k}/2 \end{aligned} \qquad (6)$$

using sgn(x) the sign function: sgn(x)= –1 if x<0, and sgn(x)= 1 otherwise.

Similarly, equation (2) and condition (3) leads to

$$\begin{aligned} N(k) = N_i(k) &+ 0.5 \\ &- 0.5\operatorname{sgn}\left(\tau(k) + N_i(k)T_{D,k} - T_R\right). \end{aligned} \qquad (7)$$

III. Closed Loop Model

For the closed loop model we need to compute the output of phase accumulators and fractionnal error correction ε. Expression of reference phase accumulator is simply given by the well-known relation

$$\phi_R[k+1] = \left(\phi_R[k] + FCW\right) \bmod [2^R] \qquad (8)$$

where we take care of modulo effect resulting of the finite width *R* of the reference phase accumulator.

Similarly, the undersampled output of the DCO phase accumulator, $R_V(k)$ of the finite width *D* can be written

$$\phi_D[k+1] = \left(\phi_D[k] + N[k]\right) \bmod [2^D] \qquad (9)$$

However this expression cannot be implemented without knowledge of *N(k)*. Thanks to our previous analysis, we are here able to compute *N(k)* using (7) and, therefore implement (9).

The fractionnal phase error ε can be simply modelized as the quantified version of our previous τ_{k+1}, normalized to $\overline{T}_D$, an averaged value of T_D.

A more precise model can be derived from the analysis of the TDC in terms of quantified delay between rising and falling edges preceding the rising edge of F_{REF}. This model is not developped in this paper for sake of simplicity.

Other elements involved in the ADPLL are the phase error computation, the loop filter and the DCO. They are briefly described now.

The phase error is not just realized by an arithmetic additionner, according to

$$\phi_E[k] = \phi_R[k] - \phi_D[k] + \varepsilon[k] \qquad (10)$$

but by an adder with a limited width that take into account the binary-signed format and modulo effect.

The digital loop filter is implemented by its difference equation.

The DCO is modelized by equations given in [2]. For a small deviation Δf, we can use simple linearized model

$$f_{DCO}(k) = f_0 + \Delta f(k) = f_0 + OTW(k)K_{DCO} \qquad (11)$$

where f_0 is the central frequency, OTW is the oscillator tuning word at the input of the DCO, and K_{DCO} the gain of the DCO. Note that the real output of our model is directly the instantaneous frequency, delivered at rate F_{REF}, and not a time signal with that instantaneous frequency. However, we may compute the PSD of such virtual signal as described now.

IV. Spectral density computation

The objective of this section is to show how to compute the PSD from the instantaneous frequency given by the output of the behavioral model.

Let us consider f_i(t) the instantaneous frequency of an oscillator

$$f_i(t) = f_0 + \Delta f_i(t) = f_0 + \Delta f_{pp}\, g(t) \qquad (12)$$

where f_0 is the mean frequency, Δf_{pp} is the peak-to-peak deviation from f_0 and *g(t)* is a normalized frequency modulation pattern ($-1<g(t)<1$) with zero mean.

We define the instantaneous phase by

$$\theta_i(t) = \int_0^t 2\pi f_i(\tau)d\tau = 2\pi f_0 t + 2\pi\Delta f_{pp}\int_0^t g(\tau)d\tau. \qquad (13)$$

The output signal *s(t)* of the oscillator is given by

$$s(t) = \cos\left(\theta_i(t)\right) = \cos\left(2\pi f_0 t + 2\pi\Delta f_{pp}\int_0^t g(\tau)d\tau\right). \qquad (14)$$

With the assumption that $x = 2\pi\Delta f_{pp}\int_0^t g(\tau)d\tau$ is small enough so that $\sin(x) \approx x$, we obtain the first order approximation

$$\hat{s}(t) = \cos(2\pi f_0 t) - 2\pi\Delta f_{pp}\sin(2\pi f_0 t)\int_0^t g(\tau)d\tau \qquad (15)$$

after developing the cosine in (14).

The Fourier Transform of $\hat{s}(t)$ is

$$\hat{S}(f) = \frac{1}{2}\left(\delta_{f0} + \delta_{-f0}\right) + \frac{\Delta f_{pp}}{2}\left(\frac{G(f-f_0)}{f-f_0} - \frac{G(f+f_0)}{f+f_0}\right) \qquad (16)$$

where $G(f) = TF[g(t)]$.

For $f = \pm f_0$, the weight can also be computed by $1/2 - \pi\,\Delta f_{pp}\frac{1}{t_{\max}}\int_0^{t_{\max}}\int_0^t g(\tau)d\tau\,dt$.

Thereby, with (16), we can directly compute the PSD transform of the instantaneous frequency using solely the lowpass signal *g(t)*. The analysis above is continuous, but a similar analysis can be done in the discrete case. For implementation of a simulator based on our behavioral model, care must be taken on spectral aliasing, and a zeroth-order interpolation have to be used in order to increase the sampling period.

V. Simulations

The new behavioral model was implemented in MATLAB. Another conventional model was realized in VHDL and simulated in MODELSIM.

Simulations were done with two objectives to achieve:

1. Validation of the time behavioral model by comparison with results obtained by the VHDL model.
2. Study of spectral spurs linked to limit cycles and noise level due to quantization (TDC).

Examples reported below are typical results obtained using the behavioral model. Statistical analysis of performances and sensibility of the PLL will be developed elsewhere.

A. Time behavioral model validation

For both models with same set of parameters, we compare the transient behavior of the DCO output frequency when we change the frequency command word.

Fig 4 show the transient reponse of the output frequency of the ADPLL, when *FCW* is out of synthesizable range of the DCO (T1) and next (T2), when *FCW* changes between minimum and maximum value of the DCO. We observe the same behavior and settling time.

In Fig 5, we show the ADPLL locked behavior for both models (with the same scale). We note the same general behavior (frequency deviation, patterns), but also observe small differences in the limit cycle sequence because of

TDC modelisation and accuracy limitation in the VHDL simulator (1 femtosecond).

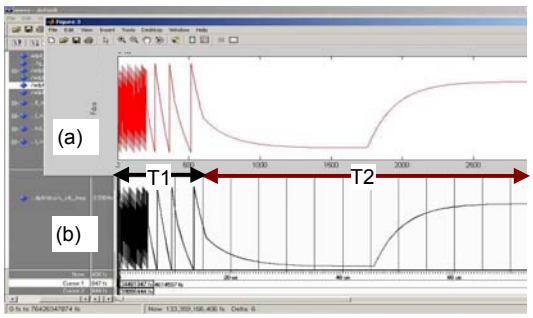

Fig 4. Simulation comparison of instantaneous frequency between new behavioral model (a) and VHDL model (b)

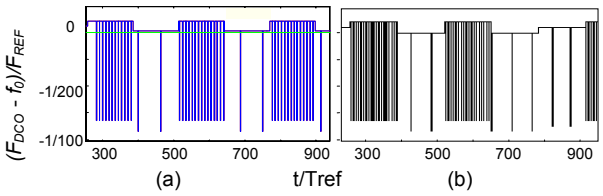

Fig 5. Limit cycle comparison between new behavioral model (a) and VHDL model (b)

B. ADPLL Locking sequence

Convergence of the ADPLL is achieved using three different modes [2]: first, a calibration (CAL) mode initiates the TDC and the central frequency of the PLL, independantly of frequency command word. Second, an acquisition (ACQ) mode acquires channel selected by FCW. Third, a tracking (TRK) mode achieves the required performances (use of a Sigma Delta modulator can further refine this last mode).

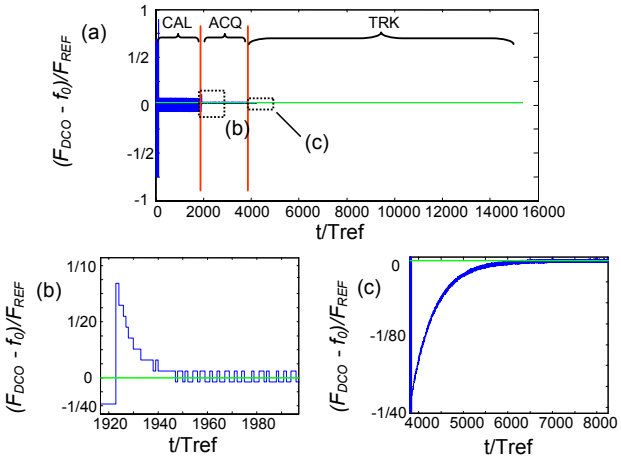

Fig 6. Locking sequence (a) and zoom (b, c) on transient at the modes shifts

Different frequency steps and gains for the DCO characterize these three modes.

The behavioral model enables to measure and analyse the locking sequence: transient parts and fluctuations during steady states as shown in Fig 6.

Moreover, comparison with same simulation time and parameters shows that the new behavioral model is 20 times faster than VHDL model with 1fs resolution.

C. Spectral density computation

With the spectral density computation analysis in section IV, we easily compute the PSD of the instantaneous frequency of the DCO.

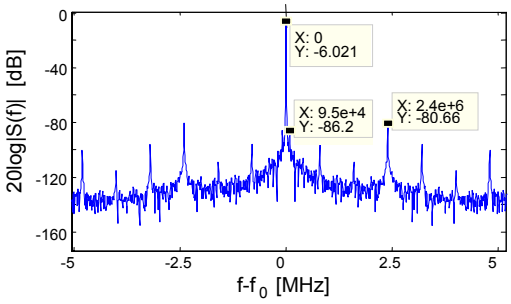

Fig 7. PSD of the locking sequence when PLL is settled

In Fig 7, we show an example of PSD when the PLL is locked. We can note the amplitudes and frequencies of spurs, due to accuracy of TDC and precision of DCO.

VI. Conclusion

We have presented a simple and effective behavioral model for an all-digital phase locked loop. This model, based on a simple expression of the delay that is an image of phase error, enables simulating the PLL at low rate (independently of carrier frequency) instead of conventional high rate simulator.

Simulation comparisons with a VHDL simulator confirm both the validity and the speed of this model.

Such a model will be used to analyse several aspects of this ADPLL and select a set of parameters optimizing its performance.

References

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