# Implantation of FIR filters on fixed-point DSP for communication systems

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## ABSTRACT

This paper describes the teaching of Digital Signal Processors and FIR filters through a practical case study on the implantation of FIR filters on fixed-point DSP (TMS320C54X) for communication systems.
The classical FIR implantation emphasizes the good optimization of this DSP architecture for symmetrical transversal FIR filters. The block filtering approach by overlap and add with FFT emphasizes on data manipulation, and FFT implantation with associated bit reverse addressing. The actual implantation of digital communication systems often involves multirate processing for efficiency reasons. This last technique is introduced with multirate polyphase implantation of the raised cosine filter.
We first introduce the general curriculum at ESIEE, then we focus on the digital communications specialization where this lab take place. Then we present the DSP lab on FIR filters for digital communications..

## 1. INTRODUCTION

The curriculum at ESIEE starts after baccalauréat and is divided into two main parts. During the first three years, the students receive lectures in mathematics, physics, foreign languages, humanities and basics on electrical engineering and especially 30h in signal processing during the third year. For the last two years, they have to choose a specialization among four possibilities : computer science, control, electronic and micro-electronic systems and finally signal processing and telecommunications. The objective of the « signal processing and telecommunications » major is to form engineers for the telecommunications sector and more specially for radio communications.
The $5^{h}$ year is dedicated to a training whether in microwaves or in digital communications. The $4^{th}$ year has for objective to offer a basic culture in the different field of telecommunications : Digital Signal Processing, Digital communications and networks, Radiocommunications and Microwaves. During this $4^{th}$ year, a 45-hour course is devoted to a case study which is a practical synthesis of the different courses. It is based on the study and the simulation of a terrestrial digital microwave link.. The students use 2 simulation software packages : Omnisys from HP-EESOF for the microwave simulation, and SPW from Cadence for the base-band digital communication study. By this way they can apprehend the different following problems :

- Link budget,
- Study of the non linearity questions through the use of a 16QAM modulation,
- Inter-symbol Interference, raised cosine shaping filter and adapted filter,
- techniques for error probability estimation : Monte Carlo and semi-analytic approach,
- Multipath channel (Rummler model) and equalization.

Bearing in mind the very fast evolution of the telecommunication standards, and the coexistence of multiple norms and modes, the implantation of the base-band processing in programmable devices such as DSP (Digital Signal Processors) is a very interesting solution for digital communication systems. This is the reason why, this case study includes the study of the implantation of algorithms on fixed-point DSP in addition to the simulation and performance analysis aspects. Of course, for simplicity reasons, the used sampling rate for that part of the case study is much smaller than the one that would be necessary for the actual microwave link.
For this study, we have chosen to focus on Finite Impulse Response (FIR) filters implantation, and under the circumstances on the raised cosine filter.

### THE TMS 320C542

The chosen DSP for this work is the TMS320C541 [1]. The TMS320C541 is a DSP of the last generation of the 16 bit fixed-point DSP, oriented in particular, towards mobile digital communications applications. The architecture of this device is based on a Harvard architecture built around a program bus, 2 data busses for reading and 1 data bus for writing. This enables the existence of a specialized instruction for FIR filters. The data paths allows the 16x16 multiplication-accumulations (MAC) with results on 40 bits, the 8 guard bits enabling 256 MAC without

overflow. The DSP contains special hardware for Viterbi algorithm computations. The efficient implantation of algorithms requires both a good ordering of computations and an efficient memory organization and management. Signal processing algorithms are characterized by an important data flow. We will see how the proposed study allows to better understand the importance of these aspects of algorithms implantation especially through circular addressing techniques..

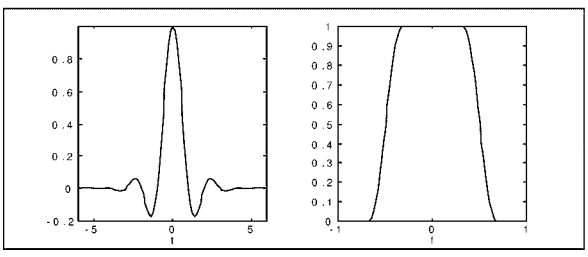
### THE SHAPING FILTER

The transmission channels are always band limited, because of physical constraints or because of operating reasons (limitation of co-channel interference for example). In practice, it is necessary to limit the bandwidth of the transmitted signals and this bandwidth limitation, most of the time, leads to InterSymbol Interferences (ISI). The adequate shaping of the transmitted pulses allows to use efficiently the available channel bandwidth while preserving a sampling instant where ISI is null. Such a good pulse shaping can be realized by raised cosine filters. Their impulse response is given by :

$$h(t) = \mathrm{sinc}\left(\pi t / T\right)\frac{\cos\left(\pi\beta t / T\right)}{1-\left(4\beta^2 t^2 / T^2\right)}$$

where β is the roll-off factor that determines the excess bandwidth relative to the Nyquist bandwidth (which is the minimum possible bandwidth enabling the zeroing of ISI and which is equal to 1/2T for a symbol rate of 1/T).

In the case study, the coefficients of the FIR raised cosine filter are calculated for a roll factor equal to 0.35. The over-sampling ratio is equal to 8. In order to obtain the desired out of band attenuation, 97 coefficients are necessary (the filter length is 12 symbols).



### THE EXPERIMENTAL CONDITIONS

The case study uses the following equipment :

- a PC with an evaluation board for the C541 (EVMC54X),
- a digital oscilloscope

A basic program is given to the students. It includes :

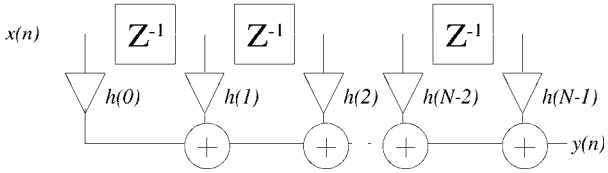
- the drivers for the analog interface device (AIC) of the EVM board which is programmed to work at a sampling frequency of 9600 Hz.
- A routine generating a sequence of pseudo random symbols at 1200 bauds with a rectangular shaping. This sequence is obtained through the generating polynomial $P(x)=x^{15}+x^{13}+x^{9}+x^{8}+x^{7}+x^{5}+1$. The routine is scheduled on the AIC interruption (9600 Hz). The given program sends the pseudo-random sequence to the AIC, and the output of the digital to analog converter is connected to the oscilloscope. For the students, the first task consists in synchronizing the scope to obtain an eye diagram with a rectangular pulse (this does not generate any particular problem because the scope synchronizes itself on the zero-crossings of the signal which due to the rectangular shaping are not distorted). After the introduction of a raised cosine pulse shaping, the zero-crossing are strongly distorted and it is no more possible to directly visualize an open eye diagram on the scope. It is then necessary to insert a rate synchronization. In this study, this rate synchronization is simulated in the routine generating the pseudo-random sequence where the state of the DSP XF (eXternal Flag) pin is changed at each new symbol. The XF pin is available on the connector HE10 of the EVM board. This signal is then used as synchronization for the scope. This last precision suggests that the program could also be adapted to study the performances of algorithms for timing recovery.

## 2. TRANSVERSAL IMPLANTATION

The convolution equation for a FIR filter is given by :

$$y(n) = \sum_{k=0}^{N-1} h(k)x(n-k)$$

The implantation of such a filter can be done with a transversal structure (see next figure) :




This structure is the more direct. It uses only 2 busses for the coefficients and 1 bus for the data. The result of each multiplication is accumulated in one of the two 40-bit accumulators (ACCU). This implantation requires N multiplications and N-1 additions for each output sample. The storing and refreshing of the

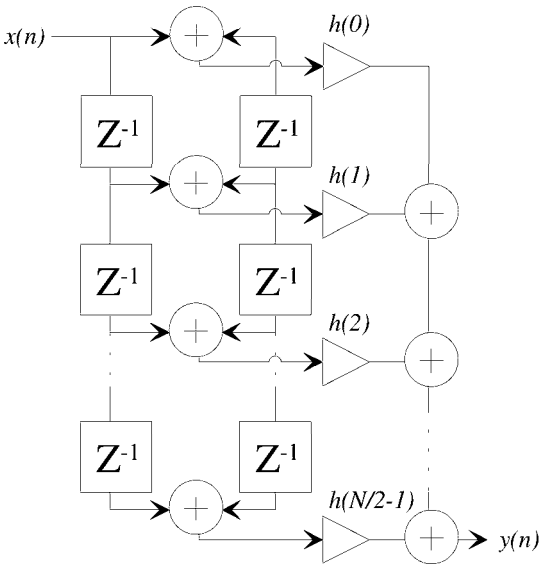
internal data can be efficiently realized by a circular buffer, which suppress the necessity of copying N-1 memory places. The pedagogical interests of this first approach consist in:

- the development of a compact program using the repetition of instructions (RPT, RPTZ),
- the understanding of memory organization by the implantation and comparison of 2 different techniques for memory management for the filter data (DELAY et circular addressing),
- the presentation of the computation noise and of the interest of architectures limiting this noise.

## 3. SYMETRICAL FILTER IMPLANTATION

The impulse response of raised cosine filters is symmetrical. FIR filters are very often used in digital communications in order to realize linear phase filters. This linear phase property leads to a symmetry of filter coefficients, *h(k)=h(N-1-k)* that enables to write the filtering equation in the following way, when the number of coefficients is even :

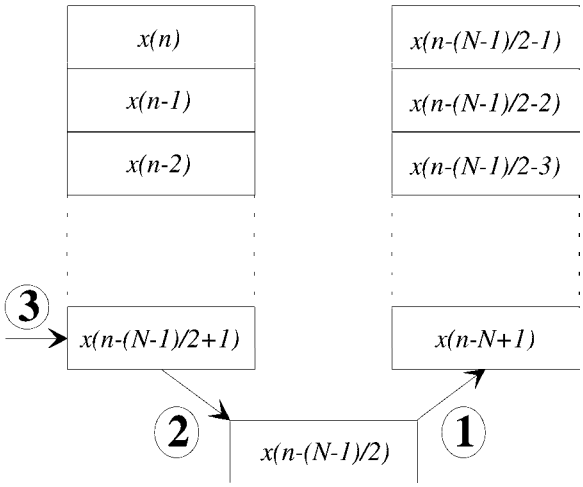
$$y(n) = \sum_{k=0}^{(N/2)-1} h(k)\left(x(n-k) + x\left(n-(N-1-k)\right)\right)$$




When the number of coefficients is odd (which is the case here with 97 coefficients) the central coefficient corresponds to the current symbol and the equation is :

$$y(n) = x\left(n-(N-1)/2\right) + \sum_{k=0}^{((N-1)/2)-1} h(k)\left(x(n-k) + x\left(n-(N-1-k)\right)\right)$$

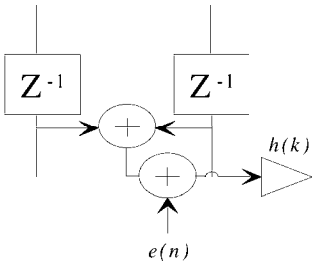
The fact that the number of coefficients is odd, implies a memory organization with 3 blocks. The first one is the half-buffer corresponding to the terms *x(n-k)*, the second half-buffer corresponds to the terms *x(n-(N-1-k))*, and the third block is the central sample. Each of the 2 buffers is ruled as a circular buffer.




The bold numbers indicate the sequencing order of the processing.

The direct realization of the above equation requires a triple access to the memory : 2 data accesses and 1 coefficient access, the coefficients are then placed in program memory. A special attention must be given to the memory organization since in the case of a double operand memory (Xmem and Ymem) the number of the possible types of addressing is reduced in order to make it possible to code the instruction on 16 bits.

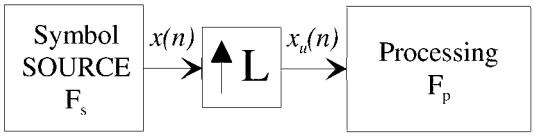
The number of operations if one selects this type of implantation is then of N/2 additions to combine the samples on which apply the same coefficients, followed of N/2 multiplications and finally N/2-1 additions. That is coarsely, N additions and N/2 multiplications. The number of multiplications was thus divided by two compared to the traditional transversal structure. This profit is however made to the price of the introduction of a quantification noise, e(n), between the output of the adder and the input of the multiplier by the coefficient.



Indeed in the data path of data of the TMS320C54X, the result of the first addition is stored in the high part of accumulator A, A(32-16). This 16-bit word is then multiplied by the coefficient pointed by the address in the program memory. If one takes as convention that data belong to the interval [ - 1,1 ], then they will have to be coded in Q14 (14 fractional bits) before the addition so that the result does not give place to an overflow. The introduction of this quantification noise is then the price to pay to divide by two the number of processor cycles for the evaluation of each output sample.

## 4. MULTIRATE IMPLANTATION

In the application which occupies us, the symbol rate (Fs) is lower or equal to the frequency of processing (Fe), corresponding to Fs multiplied by the number of samples per symbol, i.e. the over-sampling factor (L). the data processing sequence can then be represented as in the figure below:




The processing in our case corresponds to the calculation of the output of the filter. This calculation will thus be made with an input $x_u(n)$ where L-1 over L samples are equal to 0. This type of situation is relatively frequent in digital communications base-band processing, where the different algorithms require a more or less significant number of samples per symbol. In this case study, the symbol rate is equal to 1200 bauds and the sampling frequency, i.e. the update rate of the output of the filter, is 9600 Hz. There are thus 8 samples per symbol. The multirate approach and the polyphase decomposition of the filter will enable to significantly reduce the number of calculations to be carried out per sampling period for the evaluation of the filter output. The multirate approach that we will use here rests on the following remarkable relations :


On the diagram on the left, the filter is calculated at the frequency $L.F_s = F_P$, then on the diagram of the right part the filter is evaluated at the frequency $F_s$ and its output is then over-sampled at frequency $F_P$.
The first stage of this approach thus consists in decomposing the filter in a polyphase form, i.e. to decompose the transfer function H(z) in polynomials of $z^L$ on which it is then possible to apply the above remarkable relation. The polyphase decomposition of the type I is most direct to derive. If N is the length of the impulse response and L the over-sampling factor, one must have N=mL with m whole. The Z transform of the impulse response is then written:

$$H(Z) = \sum_{n=0}^{mL-1} h(n) Z^{-n},$$

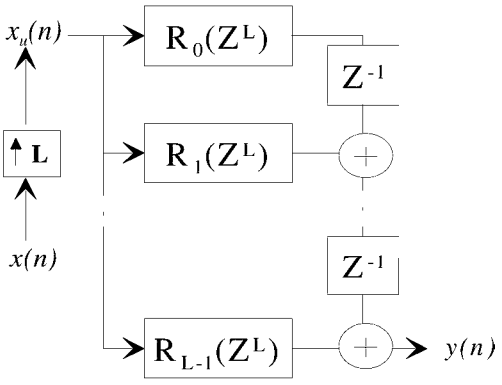
If one changes the variable $n = pL + k$ with $0 \le k \le L-1$ and $0 \le p \le N/L-1$, then one obtains the expression of the polyphase decomposition of type I :

$$H(Z) = \sum_{k=0}^{L-1} Z^{-k} \sum_{p=0}^{N/L-1} h(pL+k)\left(Z^L\right)^{-p}$$
$$= \sum_{k=0}^{L-1} Z^{-k} E_k\left(Z^L\right),$$

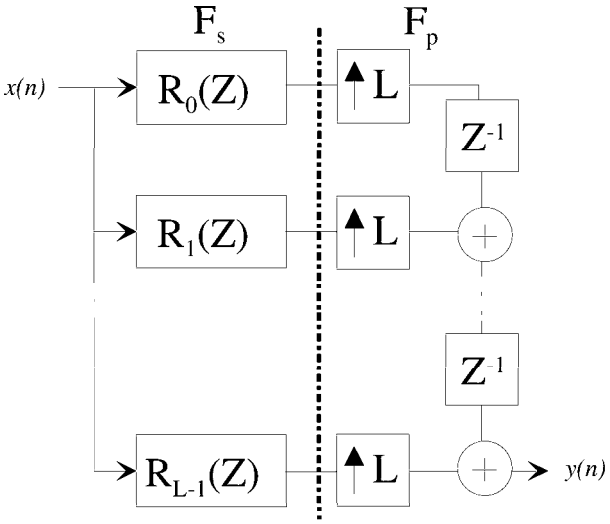
with $e_k(p) = h(pL+k)$.
The type II polyphase decomposition is obtained in changing the variable $n = pL + L - 1 - k$ :

$$H(Z) = \sum_{k=0}^{L-1} z^{-(L-1-k)} R_k\left(z^L\right),$$

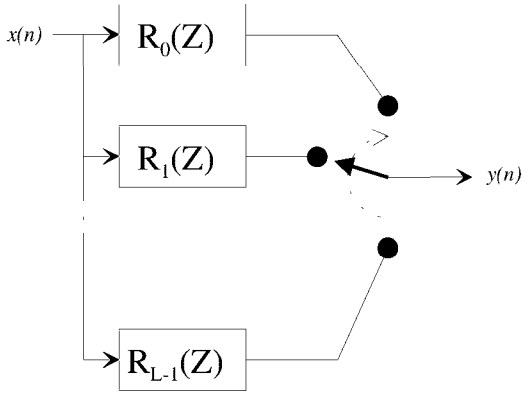
with $r_k(p) = h(pL + L - 1 - k)$.
This second decomposition is represented on the figure below. The processing is decomposed on L-1 parallel units. Each unit calculates at each sampling period the output of a FIR filter of length N/L instead of N. Each $R_k(z^L)$ is a polyphase component. The impulse response of $R_k(z^L)$ is derived by sub-sampling the initial filter impulse response. All the processing is done at the highest sampling frequency $F_P$.




By using the remarkable relation one obtains the following synoptic:




In this schematic diagram each polyphase component is evaluated at the lowest frequency $F_S$. The output structure (on the right of the diagram) which corresponds to the cascade of the interpolators (oversampling) followed by the chain of delays allows us to introduce the formalism of the switch which very convenient for an implantation on a microprocessor. By examining the right part of the diagram, one observes that, at one given time $kT_p$, only one output of the polyphase components after over-sampling is non zero. At k=0, only the output of component $R_{L-1}$ will be non null; with k=1, it will be component $R_{L-2}$; and finally with k=L-1 it will be the component $R_0$ , the index k being incremented at the frequency $F_P$, this suggests that, at every instant $kT_p$, one evaluates the output of only 1 polyphase component, instead of the complete initial filter. This reduces the calculation load by a factor L, compared to the classical approach. Here, for each sampling period $T_p$, one evaluates the output of a filter of length N/L , i.e. N/L multiplications and N/L-1 additions, instead of N/2 multiplications and N additions if only the symmetry of the coefficients is exploited. The gain in number of operation increases with the oversampling factor. The following synoptic presents the model of the switch.



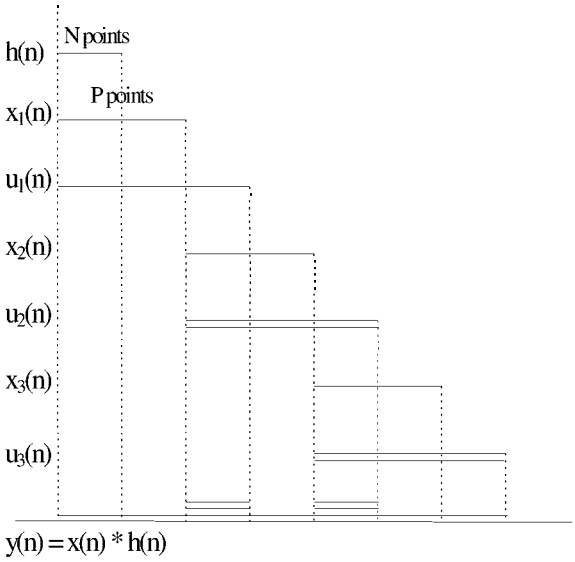

The processing of the shaping filter can then be scheduled by the interruption corresponding to the sampling rate $F_P$. With each interruption, one decrements modulo L a counter initialized with L-1, The value of the counter corresponding to the index k of the polyphase component to evaluate.
It should be stressed that this type of approach will be extremely beneficial in the case of realization of very narrow band FIR filter, because the over-sampling factor could be very significant in that case.

## 5. BLOCK FILTERING WITH FFT

The number of operations which were given for the methods presented until now, corresponded to the calculation of one output sample. If now one considers in input a length-P vector for example, then in the transversal case, the number of multiplications and additions necessary is equal to NP.
If one uses simulation tools such as SPW, HP-ADS or Ptolemy to evaluate the performances of a communication system, the cost of calculation and thus the time of simulation can become very significant. And those software packages offer a method of filter calculation in the frequential domain, which can benefit of the efficiency of the FFT algorithm and makes it possible to reduce in an extremely significant way the duration of simulation. The implantation of filters that work on blocks of input samples in the frequential domain, also make it possible to obtain equalizers whose convergence performances can be higher than equalizers working sample by sample.
The basic idea for frequential implantation of a FIR filter is to calculate the filter output block by block of M samples and to use the convolution theorem which says that the Discrete Fourier Transform (DFT) of a the circular convolution of 2 sequences and of length M is the product of the DFT of the 2 sequences.
First we will explain how block filtering works and second how it can be realized using FFT.

### BLOCK FILTEREING BY THE OVERLAP-ADD METHOD :

Suppose the impulse response h(n) has a length N.
The long input sequence x(n) is split in small successive blocks of P samples $x_k(n)$. The output of the filter corresponding to each block of size P, is a block $u_k(n)$ of size P+N-1 samples. The final output of the filter is obtained by overlapping and adding the outputs corresponding to the successive input blocks.




**CALCULATING THE SUCESSIVE CONVOLUTIONS BY FFT :**

The successive linear convolutions $u_k(n)=x_k(n)*h(n)$ can be calculated buy FFT in the following way.

Let M be a power of 2 bigger than N+P-1. The 2 sequences $x_k(n)$ and h(n) are zero padded in order to obtain 2 sequences of equal length M. The circular convolution of the zero-padded sequences coincides for its N+P-1 first samples with the linear convolution of the original sequences. So the linear convolution of the 2 sequences h(n) and $x_k(n)$ can be obtained by :

- Calculating the FFT of the 2 zero-padded sequence of length M ,
- Multiplying the 2 FFT,
- Taking the inverse FFT of the product sequence,
- keeping only the P+ N-1 first points of the result.

In practice the FFT of h(n) has to be calculated only once at the beginning of the processing. So the resulting computation load is equal to the calculation of 1 FFT plus 1 IFFT plus the product of two M points FFT sequences. This globally corresponds to : $4M\log_2(M)$ real multiplications and $6M\log_2(M)$ real additions plus 4M real multiplications. These values must be compared to the number of operations necessary for the calculation of P output samples with the transversal structure : NP multiplications and additions.

So the block frequential structure is interesting if :

$PN > 4\,(P+N-1)\,(1 + \log_2(P+N-1))$

The value N is fixed but P can be arbitrarily chosen. For example for M = 1024, the calculation load is divided by 2 with this method.

However the implantation in the frequential field introduces many constraints especially concerning the filter group delay which is then increased of the acquisition time of an input data block. The frequential implantation is also extremely constraining from the point of view of the organization of the data. Finally one can say that in the case of a fixed point DSP, if the frequential method can decrease the number of operations, it, on the other hand, presents the disadvantage of introducing calculation noise due to the FFT.

## 6. CONCLUSIONS

We have presented a DSP lab consisting in the implantation on fixed-point DSP of different structures of FIR filters for digital communications.

In a limited amount of time, the students can realize a real-time actual system, from which they can observe different signals on an oscilloscope, and particularly an eye diagram.

This work allows them to synthesize several topics in digital signal processing and to learn new concepts on digital signal processors and real time systems.

The main technical acquisition are :

- Training on TMS320C541 in a real environment : they use the CPU, different types of addressing modes, they manipulate interruptions, they use the standard serial port to which the analog converter is connected, they use the circular buffers.
- Implantation of digital filters with fixed point DSP, comparison of the efficiency of different structures from the point of view of the calculation load and of the introduced calculation noise.

## ACKNOWLEDGEMENTS

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## REFERENCES

[1] *TMS320C54X User's guide, Texas Instruments Inc., 1997.*

[2] Porat B., *A course in Digital Signal Processing,* John Wiley and Sons, Inc., 1997.