Series-Parallel Charge Pump Conditioning Circuits for Electrostatic Kinetic Energy Harvesting

Armine Karami, *Student Member, IEEE*, Dimitri Galayko, *Member, IEEE*, and Philippe Basset

***Abstract*—This paper presents a new family of conditioning circuits used in electrostatic kinetic energy harvesters (e-KEHs), generalizing a previously reported conditioning circuit known as the Bennet's doubler. The proposed topology implements a conditioning scheme described by a rectangular charge-voltage cycle (QV-cycle) of tunable aspect ratio. These circuits show an exponential increase of the converted energy over operation time if studied in the sole electrical domain. The QV-cycle's aspect ratio can be set to values that were previously inaccessible with other exponential conditioning circuits. After a brief intuitive presentation of the new topology, its operation is rigorously analyzed and its dynamics are quantitatively derived in the electrical domain. In particular, the aspect ratio of the rectangular QV-cycle describing the biasing scheme of the transducer is expressed as a function of the circuit's parameters. Practical considerations about the use of the reported conditioning circuits in actual e-KEHs are also presented. These include a discussion on the applications of the proposed conditioning, a description of the effects of electrical nonidealities, and a proposition of an energy extracting interface.**

***Index Terms*—Conditioning circuits, electrostatic kinetic energy harvesting, energy conversion, series-parallel charge pumps.**

I. Introduction

CONDITIONING circuits are a critical block of electrostatic kinetic energy harvesters (e-KEHs). Indeed, an inherent property of the electrostatic transduction mechanism is that the harvested power depends on the biasing scheme of the transducer throughout the variation of its capacitance between two extremal values. This biasing scheme depends on the used conditioning circuit.

Until now, several topologies for e-KEHs conditioning circuits have been studied, realizing different biasing schemes. The requirement for electrical interfaces that are self-synchronized with the external vibrations have legitimated the study of a family of "charge-pump" conditioning circuits, e.g., [1]–[3]. Circuits of this family have the common fundamental characteristic of implementing a rectangular charge-voltage diagram at each cycle of the conditioning circuit's operation (rectangular QV-cycle) [4]. The QV-cycle is a simple and powerful geometrical tool that summarizes the evolution of the transducer's biasing and charge during a cycle of its capacitance variation [5], [6]. It gives a quick estimation of the converted energy per cycle, which is equal to the area enclosed by the transducer's QV curve.

Manuscript received April 16, 2016; revised August 7, 2016; accepted August 21, 2016. Date of publication October 12, 2016; date of current version January 6, 2017. This paper was recommended by Associate Editor N. Krishnapura.

A. Karami and D. Galayko are with Sorbonne Universités, UPMC Univ Paris 06, UMR 7606, LIP6, F-75005 Paris, France (e-mail: armine.karami@lip6.fr).

P. Basset is with Université Paris-Est, ESYCOM, ESIEE Paris, France.

Digital Object Identifier 10.1109/TCSI.2016.2603064

As shown in [4], a fundamental characteristic of these charge-pump conditioning circuits is that the amount of converted energy at each cycle of the capacitance variation is a function of the internal energy in the circuit and of the transducer capacitance variation.

All the cited charge-pump conditioning circuits exhibit an optimal cycle in terms of the harvested energy per cycle (that will be referred to as harvested power in the rest of the paper). With these circuits, the harvested power is fundamentally limited by the transducer's capacitance variation and the initial energy stored in the circuit. Moreover, under autonomous operation of the circuit submitted to a variation of the transducer's capacitance, the harvested energy is reinvested in the circuit, changing the harvested energy at the next cycle. Notably, after reaching an eventual maximum in the harvested power, the converted energy per cycle of the capacitance variation tends to zero, i.e., the QV-cycle degenerates into an horizontal line.

In [7], De Queiroz *et al.* present a new circuit of the charge-pump conditioning family, that is referred to in the literature as the "Bennet's doubler," as it is derived from an electrostatic machine first described by Bennet *et al*. in the 18th century [8]. This charge-pump conditioning circuit has the major advantage of exhibiting an operation mode in which the harvested power is exponentially growing, and a fortiori non-saturating, as long as the electromechanical coupling is not taken into account. This exponential growth starts from an arbitrarily low initial energy in the system.

In the present paper, a new generic conditioning circuit topology, based on a series-parallel charge pump topology, is presented and rigorously analyzed in the electrical domain. This topology is shown to be a generalization of the Bennet's doubler, uncovering an entire new family of conditioning circuits. The full rigorous analysis of the Bennet's doubler is hence contained in the presented analysis. This generic topology allows the realization of different biasing schemes of the transducer at the scale of one cycle of the transducer's capacitance variation (i.e., different QV-cycles), with long-term autonomous exponential increase of the harvested power. The proof of the exponential operation mode and the quantitative derivation of the associated QV-cycle's geometric properties is the subject of the analysis. As it is discussed in the final part of the paper, this variety of conditioning schemes can be of interest, for example in the case of electret e-KEHs, or to optimize the device's operation under the impact of the electromechanical coupling, that is dependent on the biasing scheme implemented at each cycle of the transducer's capacitance variation.

The plan of the paper is as follows. In Section II, a simplified and intuitive way to describe the original Bennet's doubler circuit is presented, and based on this view of the circuit, the generic circuit topology is naturally deduced. In Sections III

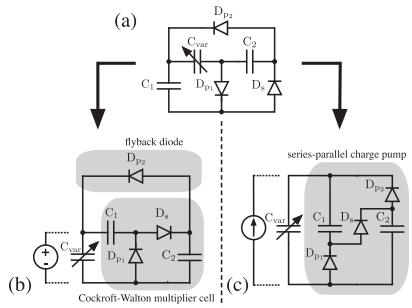

Fig. 1. Different representations of the Bennet's doubler circuit. The original representation is depicted in (a). The topology as represented in (b) has been proposed in [9]. The reasoning in the present work is based on the circuit viewed as in (c).

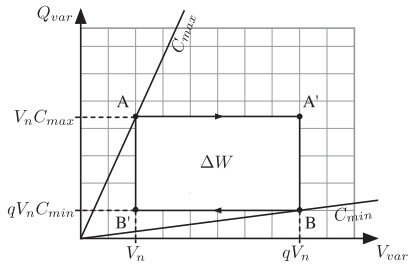

Fig. 2. QV-cycle for an e-KEH with a charge pump conditioning circuit that implements a fixed ratio q between the voltages biasing the transducer at its extremal capacitance values.

and IV, the topology is formally analyzed to quantitatively describe the circuit's dynamics and its different operation regimes, submitted to a periodic variation of the transducer's capacitance. Finally, considerations about the practical use of this circuit in an e-KEH context are discussed in Section V: the QV-cycle of the circuit is derived, motivations for the use of the presented topology are given, and generic energy extracting interfaces are discussed.

II. Presentation of the Circuit

The original Bennet's doubler conditioning circuit is depicted in Fig. 1(a). The variable capacitor $\mathrm{C_{var}}$ models the transducer electrically, and is varying over time between fixed maximal and minimal values (not necessarily periodically). Note that, as the paper deals with the analysis in the sole electrical domain, $\mathrm{C_{var}}$ is considered in this study as an unalterable input. The biasing scheme implemented by this circuit, in the steady-state regime, is such that the e-KEH has the property of control-less exponential increase of the harvested power, as discussed in the introduction. This is true as long as the ratio between maximal and minimal capacitance values is larger than 2. This exponential increase and the condition on the transducer's extremal capacitance values are fundamentally due to the rectangular QV-cycle of the circuit which exhibits a *fixed* ratio of 2 between the extreme voltages across the transducer at the scale at one cycle throughout the circuit's operation. At any cycle of its operation in the exponential steady-state mode, the QV-cycle of the Bennet's doubler circuit is therefore as depicted in Fig. 2, with $q = 2$.

In [9], Lefeuvre *et al.* have proposed to view the Bennet's doubler conditioning circuit as a voltage doubling cell, as depicted in Fig. 1(b), to which a flyback diode is added between the output capacitor and the variable capacitor. From this

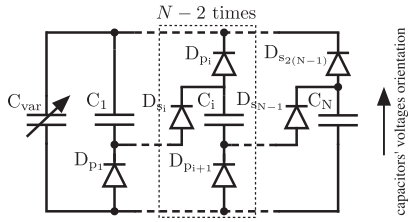

Fig. 3. The proposed generic topology for series-parallel charge-pump conditioning circuits of e-KEHs.

representation of the circuit, it comes that adding Cockcroft-Walton multiplier cells in the flyback enables to modulate the biasing of the circuit's capacitors, as explained in [10]. This is the first generalization of the Bennet's circuit. Indeed, it shows the same control-less exponentially-growing voltage in its steady-state operation regime, as it implements at each cycle of the capacitance variation, an extreme voltage ratio tending to q, which is such that $1 < q = (K+1)/K \leq 2, K \in \mathbb{N}^*$, where K is the number of multiplier cells in the flyback.

In the present paper, to have a grasp of its operation principle, it is proposed to first view the Bennet's doubler circuit as a series-parallel voltage multiplier, driven by an alternating current source modeling the transducer, as depicted in Fig. 1(c). The circuit cyclically alternates between two phases of positive and negative current. In phase (i), the current is positive and the fixed capacitors of the network are in series through D_s. At the end of this phase *each one* of the capacitors has received a charge δQ. In phase (ii), the current is negative, and the fixed capacitors of the network are in parallel with the current source through D_{p_1} and D_{p_2}. The *total* charge given back to the current source is equal to δQ. Thus, at the end of the cycle, the total charge in the fixed capacitors C_1, C_2 has increased of δQ. Consequently, the system's total energy has increased. If the ratio between δQ and the total charge in the circuit's capacitors at the beginning of the corresponding cycle is fixed throughout the circuit's operation, then the system's total energy increases exponentially over the cycles.

Viewing the variable capacitor as a voltage or a current source driving the fixed capacitor network only serves as an intuitive description of the circuit's operation based on traditional widely-used series-parallel switched capacitors networks. In point of fact, it is necessary to describe the transducer's biasing evolution locally across one cycle of the capacitance variation (e.g., in terms of its QV-cycle) to derive the resulting long-term dynamics of the circuit, and to identify its different operation regimes. Therefore, a rigorous analysis has to be carried out replacing the current source by the transducer's variable capacitor, C_{var}. The fundamental law $Q_{\mathrm{var}} = V_{\mathrm{var}} C_{\mathrm{var}}$, is then responsible for the circuit's dynamics subsequent to C_{var}'s variation.

The generic series-parallel conditioning circuit topology proposed in this paper is depicted in Fig. 3. It is a natural generalization of the circuit represented in Fig. 1(c) to a number of fixed capacitors branches greater than 2. It is shown in the rest of the paper that at the scale of one cycle, the extremal values of the bias across the transducer have a fixed ratio equal to some rational q, that is set by the choice of the circuit's elements. The implemented QV-cycle is depicted in Fig. 2. In this mode, the harvested power increases exponentially.

The two next sections go through a full and rigorous analysis of the circuit's operation. The conditions for the circuit to

operate in the exponential mode, and the relations between the parameters and the circuit's dynamics, are derived. This operation mode is the most advantageous in the electrical domain, as it allows to reach high energy conversion rates, instead of a converted energy tending to zero for long times for saturating modes. The different possible steady-state operation regimes of the generic circuit are described. Note that, in the process, this completes the analysis of the Bennet's doubler, which is a particular case of the generic topology, for which only the exponential regime has been studied so far.

III. Local Evolution Laws

The following analysis of the circuit's dynamics presumes that $C_{\rm var}$ is monotonously varying between fixed minimum and maximum, that will be denoted $C_{\rm min}$ and $C_{\rm max}$, respectively ($C_{\rm max} > C_{\rm min}$). The parameter η is defined as:

$$\eta = C_{\rm max}/C_{\rm min}. \tag{1}$$

A cycle is defined as a variation of $C_{\rm var}$ between a local maximum or minimum to the following local maximum or minimum. The purpose of this subsection is to give the evolution law of the circuit's capacitors voltages from an arbitrary cycle to the next.

The voltage across $C_{\rm var}$ will be denoted $V_{{\rm var},\overline{n}}$ at a cycle n when $C_{\rm var} = C_{\rm max}$, $V_{{\rm var},\underline{n}}$ at a cycle n when $C_{\rm var} = C_{\rm min}$, and $V_{\rm var}(t)$ at any time t. Similarly, the voltage across a capacitor $C_i, i \in [\![1; N]\!]$, will be denoted $V_{i,\overline{n}}$ at a cycle n when $C_{\rm var} = C_{\rm max}$, $V_{k,\underline{n}}$ at a cycle n when $C_{\rm var} = C_{\rm min}$, and $V_i(t)$ at a any time t.

The chosen convention for the chronology is such that $C_{\rm var} = C_{\rm min}$ at the cycle n, then $C_{\rm var} = C_{\rm max}$ at the cycle n, then $C_{\rm var} = C_{\rm min}$ at the cycle $n+1$, and so on. Also, $t_{\overline{n}}$ denote the time when at cycle n, $C_{\rm var} = C_{\rm max}$ and $t_{\underline{n}}$ denotes the time when at cycle n, $C_{\rm var} = C_{\rm min}$. Thus, $t_{\underline{n}} < t_{\overline{n}} < t_{\underline{n+1}} < t_{\overline{n+1}}$. The cycle indexes are chosen as integers, the beginning of time is noted t_0.

All the circuit elements are considered ideal. In particular, the diode elements follow the ideal diode current-voltage law, with a zero threshold voltage.

Let's immediately note that, from the circuit topology

$$\forall\, t \geqslant t_0,\, \forall\, i \in [\![1; N]\!], V_i(t) \leqslant V_{\rm var}(t) \leqslant \sum_{j=1}^{N} V_j(t). \tag{2}$$

A. Half-Cycle: Decreasing Variable Capacitance

Let's consider an arbitrary cycle n, at the moment when $C_{\rm var}$ starts to decrease from $C_{\rm max}$ of the previous cycle n, to $C_{\rm min}$ of the cycle $n+1$.

Suppose that

$$V_{{\rm var},\overline{n}} > 0, \exists j \in [\![1; N]\!], V_{j,\overline{n}} > 0,\, \forall\, i \in [\![1; N]\!], V_{i,\overline{n}} \geqslant 0. \tag{3}$$

As no current flows until a subset of the $(D_{s_i})_{1 \leqslant i \leqslant N-1}$ diodes conduct, the law for $V_{\rm var}(t)$, immediately after $C_{\rm var}$ starts to decrease, is, for a certain $t_{\overline{n},s} \in [t_{\overline{n}}; t_{\underline{n+1}}]$

$$\forall\, t \in [t_{\overline{n}}; t_{\overline{n},s}],\ V_{\rm var}(t) = V_{{\rm var},\overline{n}} \frac{C_{\rm max}}{C_{\rm var}(t)} \tag{4}$$

and the voltage across the fixed capacitors remains constant

$$\forall\, i \in [\![1; N]\!],\ \forall\, t \in [t_{\overline{n}}; t_{\overline{n},s}],\ V_i(t) = V_{i,\overline{n}}. \tag{5}$$

1) No Series Switching: If the diodes $(D_{s_i})_{1 \leqslant i \leqslant N-1}$ do not conduct for any $t \in [t_{\overline{n}}; t_{\underline{n+1}}[$ then $t_{\overline{n},s} = t_{\underline{n+1}}$, and the voltage across $C_{\rm var}$ at the end of the half-cycle is

$$V_{{\rm var},\underline{n+1}} = \eta V_{{\rm var},\overline{n}}. \tag{6}$$

The voltage across the fixed capacitors at the end of the half-cycle is

$$\forall\, i \in [\![1; N]\!], \quad V_{i,\overline{n}} = V_{i,\underline{n+1}}. \tag{7}$$

2) Series Switching: Otherwise, the circuit will switch to its series configuration when the voltage across $C_{\rm var}$ makes the $(D_{s_i})_{1 \leqslant i \leqslant N-1}$ diodes conduct. This happens when

$$V_{\rm var}(t =: t_{\overline{n},s}) = \sum_{i=1}^{N} V_{i,\overline{n}} \tag{8}$$

and the corresponding value of $C_{\rm var}$ is

$$C_{\rm var} = \frac{V_{{\rm var},\overline{n}}}{\sum_{i=1}^{N} V_{i,\overline{n}}} C_{\rm max}. \tag{9}$$

The circuit is then equivalent to $C_{\rm var}$ being in series with a capacitor of value $C = 1/(\sum_{i=1}^{N} {C_i}^{-1})$. The voltage variation law on $C_{\rm var}$ becomes

$$\forall\, t \in [t_{\overline{n},s}; t_{\underline{n+1}}]$$

$$V_{\rm var}(t) = \sum_{i=1}^{N} V_i(t) = \sum_{i=1}^{N} V_{i,\overline{n}} + \Delta Q_n(t) \sum_{i=1}^{N} {C_i}^{-1} \tag{10}$$

where

$$\forall\, t \in [t_{\overline{n},s}; t_{\underline{n+1}}]$$

$$\Delta Q_n(t) = \frac{V_{{\rm var},\overline{n}} C_{\rm max} - C_{\rm var}(t) \sum_{i=1}^{N} V_{i,\overline{n}}}{1 + C_{\rm var}(t) \sum_{i=1}^{N} {C_i}^{-1}}. \tag{11}$$

If the circuit has entered its series configuration before $C_{\rm var} = C_{\rm min}$, the capacitors voltages when $C_{\rm var} = C_{\rm min}$ satisfy

$$\forall\, i \in [\![1; N]\!], \quad V_{i,\underline{n+1}} = V_{i,\overline{n}} + \frac{\Delta Q_n}{C_i} \tag{12}$$

where ΔQ_n is the amount of charges given by $C_{\rm var}$ to the other capacitors, from $C_{\rm var} = C_{\rm max}$ to $C_{\rm var} = C_{\rm min}$. For every capacitor of the loop, this amount is equal to

$$\Delta Q_n = C_{\rm min} \frac{\eta V_{{\rm var},\overline{n}} - \sum_{i=1}^{N} V_{i,\overline{n}}}{1 + C_{\rm min} \sum_{i=1}^{N} {C_i}^{-1}}. \tag{13}$$

Note that $\Delta Q_n > 0$ as the quantity in (9) is larger than $C_{\rm min}$ by the series switching hypothesis.

The N capacitors being all in series, with the chosen voltage orientations

$$V_{\mathrm{var},\underline{n+1}} = \sum_{i=1}^{N} V_{i,\underline{n+1}}. \tag{14}$$

Note that the voltages remained positive through the half cycle.

B. Half-Cycle: Increasing Variable Capacitance

Consider now an arbitrary cycle n, at the moment when $C_{\mathrm{var}} = C_{\min}$ starts to increase from $C_{\min}$ of the cycle n to $C_{\max}$ of the cycle n.

Suppose, without loss of generality, that the voltages are ordered as

$$V_{1,\underline{n}} \geqslant \cdots \geqslant V_{N,\underline{n}}. \tag{15}$$

Now, consider C_{var} increasing from $C_{\min}$ of the cycle n to $C_{\max}$ of the same cycle. As no current flows until the $(D_{p_i})_{1\leqslant i\leqslant 2(N-1)}$ diodes eventually start to conduct, the law for $V_{\mathrm{var}}(t)$, immediately after C_{var} starts to increase, is

$$\forall\, t \in [t_{\underline{n}}; t_{\underline{n},1}], \quad V_{\mathrm{var}}(t) = V_{var,\underline{n}} \frac{C_{\min}}{C_{\mathrm{var}}(t)} \tag{16}$$

where, $t_{\underline{n},1} \in [t_{\underline{n}}; t_{\overline{n}}]$.

Consider a fixed capacitor C_k. It will remain disconnected from C_{var}, until the diodes of its branch conduct. This eventually happens when $V_{\mathrm{var}}(t)$ becomes as

$$V_{\mathrm{var}}(t =: t_{\underline{n},k}) = V_{k,\underline{n}}. \tag{17}$$

The corresponding value of C_{var} is given by

$$C_{\mathrm{var}(k,n)} = \frac{V_{\mathrm{var},\underline{n}} C_{\min} + \sum_{i=1}^{k} V_{i,\underline{n}} C_i}{V_{k,\underline{n}}} - \sum_{i=1}^{k} C_i. \tag{18}$$

Then, when (17) is fulfilled, the voltage variation law on C_{var} (and for every capacitor in parallel with C_{var}) becomes

$$\forall\, t \in [t_{\underline{n},k}; t_{\underline{n},k+1}],$$
$$V_{\mathrm{var}}(t) = \frac{V_{\mathrm{var},\underline{n}} C_{\min} + \sum_{i=1}^{k} V_{i,\underline{n}} C_i}{C_{\mathrm{var}}(t) + \sum_{i=1}^{k} C_i} \tag{19}$$

with $t_{\underline{n},N+1} = t_{\overline{n}}$. This holds until another capacitor is eventually connected in parallel with C_{var}, i.e., until $C_{\mathrm{var}} = C_{\mathrm{var}(k+1,n)}$.

At $C_{\mathrm{var}} = C_{\max}$ of a given cycle, considering N capacitors and defining $p \in [\![1; N]\!]$ as the number of capacitors in parallel with C_{var} at $C_{\mathrm{var}} = C_{\max}$

$$C_{\mathrm{var}(p,n)} \leqslant C_{\max} < C_{\mathrm{var}(p+1,n)}. \tag{20}$$

Note that, as the voltages are supposed ordered as in (15), and as the voltages across the capacitors vary continuously

$$t_{\underline{n}} \leqslant t_{\underline{n},1} \leqslant \cdots \leqslant t_{\underline{n},p} \leqslant t_{\overline{n}}. \tag{21}$$

At $C_{\mathrm{var}} = C_{\max}$ of the cycle n, the voltages across the fixed capacitors that are in parallel with C_{var} are as

$$\forall\, k \in [\![1; p]\!]$$
$$V_{k,\overline{n}} = V_{\mathrm{var},\overline{n}} = \frac{V_{\mathrm{var},\underline{n}} C_{\min} + \sum_{i=1}^{p} V_{i,\underline{n}} C_i}{C_{\max} + \sum_{i=1}^{p} C_i} \tag{22}$$

and the voltages across the fixed capacitors that are not in parallel with C_{var} at $C_{\mathrm{var}} = C_{\max}$ of cycle n have not changed

$$\forall\, k \in [\![p+1; N]\!], \quad V_{k,\overline{n}} = V_{k,\underline{n}}. \tag{23}$$

The inequality $C_{\mathrm{var}(p,n)} < C_{\mathrm{var}(p+1,n)}$ comes from the hypothesis (15). Note that, under this hypothesis, at a given cycle at $C_{\mathrm{var}} = C_{\min}$, (20) is equivalent to, for the same cycle at $C_{\mathrm{var}} = C_{\max}$

$$V_{\mathrm{var},\overline{n}} = \cdots = V_{p,\overline{n}} > V_{p+1,\overline{n}} > \cdots > V_{N,\overline{n}}. \tag{24}$$

Finally, note that the voltages remained positive during the whole half-cycle.

C. Evolution Laws Across a Complete Cycle

1) No Series Switching: At an arbitrary cycle n, if the half cycle of decreasing of C_{var} from $C_{\max}$ to $C_{\min}$ is such that no series switching occurs (see Section III-A1), then

$$\forall\, i \in [\![1; N]\!], \quad \begin{matrix} V_{\mathrm{var},\overline{n+1}} = V_{\mathrm{var},\overline{n}} \\ V_{i,\overline{n+1}} = V_{i,\overline{n}}. \end{matrix} \tag{25}$$

2) Series Switching: The evolution law for the capacitors voltages at $C_{\mathrm{var}} = C_{\max}$ between two consecutive cycles n and $n+1$ can now be obtained for fixed p and given that (8) is fulfilled. Under these assumptions, with $\mathbf{V_{\overline{n}}} = (V_{\mathrm{var},\overline{n}}, V_{1,\overline{n}}, \ldots, V_{N,\overline{n}})^T$, the system's evolution is given by

$$\mathbf{V_{\overline{n+1}}} = \mathbf{A_p} \mathbf{V_{\overline{n}}} \quad \text{if } V_{\mathrm{var},\overline{n}} = \cdots = V_{p,\overline{n}} > V_{p+1,\overline{n}} > \cdots > V_{N,\overline{n}}. \tag{26}$$

The matrix $\mathbf{A_p}$, for $0 \leqslant p \leqslant N$, is defined as

$$\mathbf{A_p} = \begin{pmatrix} a_p & \cdots & a_p & b_p & \cdots & b_p \\ \vdots & \ddots & \vdots & \vdots & \ddots & \vdots \\ a_p & \cdots & a_p & b_p & \cdots & b_p \\ c_{p_{p+1}} & \cdots & c_{p_{p+1}} & d_{p_{p+1}} + 1 & \cdots & d_{p_{p+1}} \\ \vdots & \ddots & \vdots & \vdots & \ddots & \vdots \\ c_{p_N} & \cdots & c_{p_N} & d_{p_N} & \cdots & d_{p_N} + 1 \end{pmatrix} \tag{27}$$

where the coefficients are (28)–(31), shown at the bottom of the next page.

As all the $(V_{i,\overline{n}})_{1\leqslant i\leqslant p}$ are equal (to $V_{\mathrm{var},\overline{n}}$) and follow the same law at the scale of the cycle n, a reduced form of the matrix will be considered: $\tilde{\mathbf{A}}_{\mathbf{p}} \in \mathbb{R}^{(N-p+1)\times(N-p+1)}$

$$\tilde{\mathbf{A}}_{\mathbf{p}} = \begin{pmatrix} a_p & b_p & \cdots & b_p \\ c_{p_{p+1}} & d_{p_{p+1}} + 1 & \cdots & d_{p_{p+1}} \\ \vdots & \vdots & \ddots & \vdots \\ c_{p_N} & d_{p_N} & \cdots & d_{p_N} + 1 \end{pmatrix}. \tag{32}$$

Thus, (26) becomes, with $\tilde{\mathbf{V}}_{\overline{\mathbf{n}}} = (V_{\mathrm{var},\overline{n}}, V_{p+1,\overline{n}}, \ldots, V_{N,\overline{n}})^T$

$$\tilde{\mathbf{V}_{\overline{\mathbf{n+1}}}} = \tilde{\mathbf{A}_\mathbf{p}} \tilde{\mathbf{V}}_{\overline{n}} \quad \text{if } V_{\mathrm{var},\overline{n}} = \cdots = V_{p,\overline{n}} > V_{p+1,\overline{n}} > \cdots > V_{N,\overline{n}}. \quad (33)$$

IV. Steady-State Dynamics of the Circuit

From the local evolution laws, the long-term dynamics of the circuit shall now be derived. This is the evolution of the state of the conditioning circuit defined by $\mathbf{V_n} = (V_{\mathrm{var},\overline{n}}, V_{1,\overline{n}}, \ldots, V_{N,\overline{n}})^{\mathrm{T}} \in \mathbb{R}_+^{N+1}$, starting from an initial state $\mathbf{V_0}$, for a periodic variation of C_{var} maximum and minimum $C_{\max}$ and $C_{\min}$. These two quantities are incorporated into the system's parameters, allowing to consider the system as autonomous. The coordinates of $\mathbf{V_0}$ are supposed to satisfy (2), as constrained by the circuit, and (3).

The goal of this analysis is to rigorously describe the different possible operation regimes of the circuit, and in particular, to quantitatively describe the steady-state modes of operation, as a function of the circuit's parameters.

A. Case $\eta > N$

First, let's state the following lemma, that states that steady-state mode of the circuit (exponential *vs* non-exponential mode) does not depend on the order of the initial voltages, given that $\eta > N$ and (2), (3), are fulfilled:

Lemma 1 (Order of Voltages and Capacitors): Consider the circuit topology in Fig. 3. For any values of the initial voltages fulfilling (2) and (3)

$$\eta > N \Rightarrow \big(\exists n^* \in \mathbb{N},\ \forall\, n \in \mathbb{N},\ n \geqslant n^* \Rightarrow (V_{1,\overline{n}} \geqslant \cdots \geqslant V_{N,\overline{n}} \Leftrightarrow C_1 \leqslant \cdots \leqslant C_N)\big).$$

Proof: See Appendix. ■

Secondly, let's define the condition $\Omega(k)$

$$\Omega(k) := \text{“}C_{\max} + \sum_{i=1}^{k} C_i - (k-1)C_k > 0\text{”}. \quad (34)$$

Its negation will be denoted $\overline{\Omega(k)}$.

Note that the circuit switches in its series configuration for any configuration of the voltages, if and only if $\eta > N$: under the topology constraints over the voltages (2), and from (9), the condition is necessary and sufficient (necessary because of the case, $\forall i \in [\![1; N]\!], V_{\mathrm{var},\overline{n}} = V_{i,\overline{n}}$).

Consider a cycle $n > n^*$, where n^* is given by lemma 1, and a capacitor C_k. Suppose that, at $C_{\mathrm{var}} = C_{\max}$ of this cycle, the capacitors $C_1, \ldots, C_k$ are in parallel with C_{var}. As it is ensured from lemma 1 that the order of the voltages do not change for every cycle $n \geqslant n^*$, (18) can be used to ensure that a capacitor in parallel with C_{var} at a cycle $n \geqslant n^*$ will also be in parallel with C_{var} at the following cycle. Indeed, it is ensured that each capacitor label corresponds to the same capacitor for any two different cycles following n^*, as this depends on the order of the circuit's capacitors voltages because of the local hypothesis in (15). Some algebra yields:

$$C_{\mathrm{var}(k,n+1)} < C_{\max} \Leftrightarrow \Omega(k). \quad (35)$$

Therefore, for any capacitor C_k, if there exists a cycle $n_k \geqslant n^*$ such that $V_{\mathrm{var},\overline{n_k}} = V_{k,\overline{n_k}}$ and the condition in (35) holds, then for every $n \geqslant n_k$, $V_{\mathrm{var},\overline{n_k}} = V_{k,\overline{n_k}}$. Note that this implies that $C_1, \ldots, C_{k-1}$ are also in parallel with C_{var} at $C_{\mathrm{var}} = C_{\max}$ of every cycle $n \geqslant n_k$, by the property of n^* given by lemma 1.

Now, consider $p \geqslant 1$ capacitors in parallel with C_{var} when $C_{\mathrm{var}} = C_{\max}$, at a cycle $n_p \geqslant n^*$, where n^* is given by lemma 1. The case $p = 0$ is impossible as given the circuit topology, $\max_{1 \geqslant i \geqslant N} V_i \geqslant V_{\mathrm{var}}/N$.

Also, suppose that $\Omega(p)$. Thus, because of (35), for all $n \geqslant n_p$, $V_{1,\overline{n}} = V_{\mathrm{var},\overline{n}} = \ldots = V_{p,\overline{n}}$. Consequently

$$\exists n_{p+1} \in \mathbb{N} \cup \{+\infty\}, n_{p+1} > n_p, I_p := [\![n_p; n_{p+1}[\![\quad \forall\, n \in I_p \quad \tilde{\mathbf{V}}_{\overline{n}} = (\tilde{\mathbf{A}_p})^n\, \tilde{\mathbf{V}}_{\overline{0}_p} \quad \tilde{\mathbf{V}}_{\overline{0}_p} = \tilde{\mathbf{V}_{\overline{n_p - 1}}} \quad (36)$$

where $\tilde{\mathbf{A}_p}$ is given in (32), and $\tilde{\mathbf{V}}_{0_p} \in \mathbb{R}^{N-p+1}$.

For all $N, p, 1 \leqslant p \leqslant N$, the matrix $\tilde{\mathbf{A}_p}$ has 1 of algebraic multiplicity $N - p$ and $r_p \in \mathbb{R}$ of algebraic multiplicity 1 as eigenvalues. The following assumes that $r_p \neq 1$. The

$$a_p = \frac{\left(C_{\max} + \sum_{i=1}^{p} C_i\right) C_{\min} \sum_{i=1}^{N} {C_i}^{-1} + \sum_{i=1}^{p} C_i + p\,(C_{\max} - (p-1)C_{\min})}{(C_{\max} + \sum_{i=1}^{p} C_i)\left(1 + C_{\min} \sum_{i=1}^{N} {C_i}^{-1}\right)} \quad (28)$$

$$b_p = -\frac{C_{\min}(p-1)}{(C_{\max} + \sum_{i=1}^{p} C_i)\left(1 + C_{\min} \sum_{i=1}^{N} {C_i}^{-1}\right)} \quad (29)$$

$$c_{p_k} = \frac{C_{\max} - pC_{\min}}{C_k\left(1 + C_{\min} \sum_{i=1}^{N} {C_i}^{-1}\right)} \quad (30)$$

$$d_{p_k} = -\frac{C_{\min}}{C_k\left(1 + C_{\min} \sum_{i=1}^{N} {C_i}^{-1}\right)}. \quad (31)$$

eigenvalue 1 has a geometric multiplicity of $N-p$. Subsequently, $\tilde{\mathbf{A}}_p$ is diagonalizable over $\mathbb{R}$, and it comes that:

$$\mathbf{V}_{\overline{\mathbf{n}}} = \mathbf{P}_{\mathbf{p}} \begin{pmatrix} 1 & & & \\ & \ddots & & \\ & & 1 & \\ & & & {r_p}^n \end{pmatrix} \mathbf{P}_{\mathbf{p}}^{-1} \mathbf{V}_{\overline{\mathbf{0}_\mathbf{p}}} \tag{37}$$

$$r_p = \frac{C_{\min}\left(\left(C_{\max}+\sum_{i=1}^{p} C_i\right)\sum_{i=1}^{p} {C_i}^{-1} + p(\eta-p+1)\right)+\sum_{i=1}^{p} C_i}{\left(1+C_{\min}\sum_{i=1}^{N} {C_i}^{-1}\right)\left(C_{\max}+\sum_{i=1}^{p} C_i\right)} \tag{38}$$

and where $(\mathbf{P}_\mathbf{p}, {\mathbf{P}_\mathbf{p}}^{-1}, \mathbf{V}_{\overline{\mathbf{0}_\mathbf{p}}}) \in (\mathbb{R}^{(N-p+1)^2})^2 \times \mathbb{R}^{(N-p+1)}$. Hence

$$\begin{aligned} V_{\mathrm{var},\overline{n}} &= \alpha_{\mathrm{var},p}\ {r_p}^n + \beta_{\mathrm{var},p} \\ V_{k,\overline{n}} &= \alpha_{k,p}\ {r_p}^n + \beta_{k,p} \end{aligned} \tag{39}$$

with $(\alpha_{\mathrm{var},p}, \beta_{\mathrm{var},p}, \alpha_{k,p}, \beta_{k,p}) \in \mathbb{R}^4$, and $k \in [\![p+1; N]\!]$. A simple study of the $\tilde{\mathbf{A}}_\mathbf{p}$ map allows the derivation of the coefficients' expressions; the vectors $(\mathbf{v_i}^1)_{1\leqslant i\leqslant N-p}$, where $\mathbf{v_i}^1 = (v_{i_1}^1, \ldots, v_{i_{N-p+1}}^1)^{\mathrm{T}} \in \mathbb{R}^{N-p+1}$, are eigenvectors of $\tilde{\mathbf{A}}_\mathbf{p}$ associated to the eigenvalue 1

$$\begin{aligned} v_{i_1} &= \frac{1}{\eta-p} \\ v_{i_j} &= \delta_{i(j-1)},\ 1 < j \leqslant N \end{aligned} \tag{40}$$

where δ_{ij} is the Kronecker symbol. An eigenvector $\mathbf{v}^{r_p} = (v_1^{r_p}, \ldots, v_{N-p+1}^{r_p})^{\mathrm{T}} \in \mathbb{R}^{N-p+1}$ associated to the eigenvalue r_p is

$$\begin{aligned} v_1^{r_p} &= \frac{(p-1)C_N}{C_{\max}+\sum_{i=1}^{p} C_i} \\ v_i^{r_p} &= \frac{C_N}{p-1+i},\ \ 1 < i \leqslant N-p+1. \end{aligned} \tag{41}$$

Finally, it comes, (42)–(45), shown at the bottom of the page.

The steady-state behavior of the circuit can now readily be described, that is, the value of p for which $I_p = [\![n; +\infty$, and the long-term voltage evolution laws in this interval. Given the p previously fixed, three cases are discriminated:

1) Case $r_p > 1$: The variations of $(V_{\mathrm{var},\overline{n}} - V_{p+1,\overline{n}})_{n\geqslant n_p}$, using the evolution laws of in (37), are such that

$$(V_{\mathrm{var},\overline{n+1}} - V_{p+1,\overline{n+1}}) - (V_{\mathrm{var},\overline{n}} - V_{p+1,\overline{n}}) < 0 \Leftrightarrow \Omega(p+1). \tag{46}$$

Also, by virtually fixing the law (36) for fixed p, and from (42) and (43)

$$\lim_{n\to+\infty} \frac{V_{\mathrm{var},\overline{n}}}{V_{p+1,\overline{n}}} = \frac{\alpha_{\mathrm{var},p}}{\alpha_{p+1,p}} = \frac{(p-1)\ C_{p+1}}{C_{\max}+\sum_{i=1}^{p} C_i}. \tag{47}$$

In the case $\Omega(p+1)$, the limit in (47) being then strictly less than 1, $n_{p+1} < +\infty$ and $V_{p+1,\overline{n_{p+1}}} = V_{\mathrm{var},\overline{n_{p+1}}}$. Because of (35), $\forall\, n, n \geqslant n_{p+1} \Rightarrow V_{\mathrm{var},\overline{n}} = V_{p+1,\overline{n}}$. In the case $\overline{\Omega(p+1)}$, $n_{p+1} = +\infty$ as the sequence $(V_{\mathrm{var},\overline{n}} - V_{p+1,\overline{n}})_{n\geqslant n_p}$ is strictly increasing. For all $k \in [\![p+1; N]\!]$, the asymptotic value of the ratio $V_{\mathrm{var},\overline{n}}/V_{k,\overline{n}}$ is given by

$$\forall\, k \in [\![p+1; N]\!] \qquad \lim_{n\to+\infty} \frac{V_{\mathrm{var},\overline{n}}}{V_{k,\overline{n}}} = \frac{\alpha_{\mathrm{var},p}}{\alpha_{k,p}} = \frac{(p-1)\ C_k}{C_{\max}+\sum_{i=1}^{p} C_i}. \tag{48}$$

$$\alpha_{\mathrm{var},p} = \frac{(p-1)\left(\sum_{i=p+1}^{N} V_{i,\overline{0_p}} - V_{\mathrm{var},\overline{0_p}}(\eta-p)\right)}{\left(C_{\max}+\sum_{i=1}^{p} C_i\right)\sum_{i=p+1}^{N} {C_i}^{-1} - (p-1)(\eta-p)} \tag{42}$$

$$\alpha_{k,p} = \frac{\left(C_{\max}+\sum_{i=1}^{p} C_i\right)\left(\sum_{i=p+1}^{N} V_{i,\overline{0_p}} - V_{\mathrm{var},\overline{0_p}}(\eta-p)\right)}{C_k\left(\left(C_{\max}+\sum_{i=1}^{p} C_i\right)\sum_{i=p+1}^{N} {C_i}^{-1} - (p-1)(\eta-p)\right)} \tag{43}$$

$$\beta_{\mathrm{var},p} = \frac{\left(C_{\max}+\sum_{i=1}^{p} C_i\right)\sum_{i=p+1}^{N} {C_i}^{-1} V_{\mathrm{var},\overline{0_p}} - (p-1)\sum_{i=p+1}^{N} V_{i,\overline{0_p}}}{\left(C_{\max}+\sum_{i=1}^{p} C_i\right)\sum_{i=p+1}^{N} {C_i}^{-1} - (p-1)(\eta-p)} \tag{44}$$

$$\beta_{k,p} = V_{k,\overline{0_p}} + \frac{\left(C_{\max}+\sum_{i=1}^{p} C_i\right)\left(V_{\mathrm{var},\overline{0_p}}(\eta-p) - \sum_{i=p+1}^{N} V_{i,\overline{0_p}}\right)}{C_k\left(\left(C_{\max}+\sum_{i=1}^{p} C_i\right)\sum_{i=p+1}^{N} {C_i}^{-1} - (p-1)(\eta-p)\right)}. \tag{45}$$

2) Case $r_p < 1$: Note that, from (38), this case happens only if $\Omega(p+1)$. By virtually fixing the law (36)

$$\lim_{n\to+\infty} V_{\mathrm{var},\overline{n}} = \beta_{\mathrm{var},p}, \text{ and } \lim_{n\to+\infty} V_{p+1,\overline{n}} = \beta_{p+1,p}. \quad (49)$$

From (44) and (45), some algebra leads to

$$\beta_{p+1,p} > \beta_{\mathrm{var},p} \Leftrightarrow \Omega(p+1). \quad (50)$$

Subsequently, $n_{p+1} < +\infty$ and $V_{p+1,\overline{n_{p+1}}} = V_{\mathrm{var},\overline{n_{p+1}}}$

3) Case $r_p = 1$: In this case, the reduction done in (37) no longer holds, as the linear map $\tilde{\mathbf{A_p}}$ is no longer diagonalizable. The voltages increase in this case is linear. This can be seen from the Jordan reduction of $\tilde{\mathbf{A_p}}$, that leads to $\tilde{\mathbf{A_p}}^n = \mathbf{P_p}'(\mathbf{I_{N-P+1}} + \mathbf{N})\mathbf{P_p}'^{-1}\tilde{\mathbf{V}_{\overline{0_p}}}$, where $\mathbf{I_{N-P+1}} \in \mathbb{R}^{(N-P+1)^2}$ is the identity matrix, $\mathbf{P_p}' \in \mathbb{R}^{(N-P+1)^2}$ is invertible and $\mathbf{N}$ has all its coefficients equal to zero except for $\mathbf{N}_{2,1} = n$. This case is supposed to not happen in the rest of the analysis, as $r_p = 1$ will never be exactly reached in practice.

4) Summary: The steady-state mode of operation under the condition $\eta > N$ can now be defined. This is done by inductively applying the previous reasoning to $p+1$ parallel capacitors with $\Omega(p)$ being fulfilled, starting from the smallest p such that there exists a cycle following n^* where p capacitors are in parallel at the same cycle, and $\Omega(p+1)$ is fulfilled ($\Omega(2)$ is always fulfilled and $p \geqslant 1$). Defining Π as

$$\Pi := \min\left(\left\{p \in]\!]1; N[\![\mid \overline{\Omega(p+1)}\right\} \cup \{N\}\right) \quad (51)$$

the steady-state mode is defined as the circuit's operation regime where the biasing of C_{var} is implemented in the following fashion:

- C_{var} is in parallel with the capacitors $C_1, \ldots, C_\Pi$ at $C_{\mathrm{var}} = C_{\max}$ of every cycle, i.e., $V_{\mathrm{var},\overline{n}} = V_{1,\overline{n}} = \cdots = V_{\Pi,\overline{n}}$.
- The voltage across the capacitor $\mathrm{C_i}, i \in [\![\Pi+1; N]\!]$ at $C_{\mathrm{var}} = C_{\max}$ is such that the ratio $V_{\mathrm{var},\overline{n}}/V_{i,\overline{n}}$ tends to $(\Pi-1)C_i/(C_{\max} + \sum_{j=1}^{\Pi} C_j)$.
- C_{var} is in series with all the fixed capacitors $C_1, \ldots, C_N$ at $C_{\mathrm{var}} = C_{\min}$. Hence, C_{var} is biased by the sum of voltages across the fixed capacitors at $C_{\mathrm{var}} = C_{\min}$.

The time evolution of the voltages across the fixed capacitors C_{var} exhibits an exponential increase in this mode. Indeed, the voltages follow an arithmetico-geometric progression with common ratio $r_\Pi > 1$ in the steady-state mode.

The ratio q between the voltages at $C_{\mathrm{var}} = C_{\max}$ of cycle n and $C_{\mathrm{var}} = C_{\min}$ of cycle $n+1$ in the steady-state mode of operation is given by

$$q = \frac{\Pi + \frac{C_{\max} + \sum_{i=1}^{\Pi} C_i}{\Pi - 1} \sum_{i=\Pi+1}^{N} {C_i}^{-1} + C_{\max} \sum_{i=1}^{N} {C_i}^{-1}}{1 + C_{\min} \sum_{i=1}^{N} {C_i}^{-1}}. \quad (52)$$

Note that, in the case $\Pi \neq N$, this ratio is attained asymptotically as it is the result of a limit process [see (48)]. Also, this expression can be simplified at the cost of some justified approximations (see (65) below).

The converted energy during a cycle n of the steady-state operation defined above is obviously given by

$$\Delta W_n = \frac{1}{2}\left(C_{\max}\left({V_{\mathrm{var},\overline{n+1}}}^2 - {V_{\mathrm{var},\overline{n}}}^2\right) + \sum_{i=1}^{N} C_i\left({V_{i,\overline{n+1}}}^2 - {V_{i,\overline{n}}}^2\right)\right). \quad (53)$$

Again, the full expression is cumbersome, and the use of the QV-cycle in Section V-A will greatly simplify the expression of converted power (66).

Remark: The circuit's dynamics were derived for the steady-state operation mode, irrespective of the initial configuration (this is the purpose of lemma 1). In this process, the piecewise defined transient mode is described: for each region of the definition, the explicit evolution follows the laws given in (39), with proper corresponding values of coefficients $\alpha_{i,j}$ and $\beta_{i,j}$ [see (42)–(45)]. However, because of this piecewise definition, there is no simple way to derive the *explicit* evolution laws starting from initial voltage values that do not necessarily fulfill the order in (15), other than applying the evolution law that apply in each region, and checking for the intersections of voltage in the time domain that lead to a change of the definition region.

B. Case $\eta \leqslant N$

In this case, the condition of series switching at every cycle of the autonomous evolution is not necessarily verified. As a consequence, the lemma 1 does not necessarily hold, and the long-term evolution of the circuit's state depends not only on the values of the capacitors, but also on their initial voltages.

Because of that, to simplify the analysis, only the dynamics starting from a particular order of the circuit's capacitors voltages at the initial cycle will be considered. This particular configuration is the same as in the conclusion of lemma 1. As a matter of fact, Section V-D will highlight that the energy extraction mechanism can be designed in such a way that this particular configuration frequently occurs during the system's operation (see the role of the diode D_B in Fig. 6, explained in Section V-D).

Consider an arbitrary cycle n_0, chosen as the initial cycle. Consider that the conditions (2), (3) hold. The capacitors are labeled such that $C_1 \leqslant \cdots \leqslant C_N$. The circuit's capacitors voltages are supposed to verify

$$V_{\mathrm{var},\overline{n_0}} = V_{1,\overline{n_0}} \geqslant \cdots \geqslant V_{N,\overline{n_0}}. \quad (54)$$

If the initial voltages on the capacitors verify

$$\eta V_{\mathrm{var},\overline{n_0}} > \sum_{i=1}^{N} V_{i,\overline{n_0}} \quad (55)$$

then it can be verified by induction, using local laws of Section III, that the circuit switches in series for all cycles following n_0. Otherwise, the circuit shows the trivial dynamics of (25). The following supposes that (55) is fulfilled. By a variation of the lemma 1, and given the supposed order of the capacitors, the voltage ordering in (15) does not change for any $n \geqslant n_0$. Indeed, this is the case ***(b.1)*** in the proof (see

Appendix), but using the positivity of the expression (70), as it is sufficient to conclude, instead of the divergence to $+\infty$ of the series.

Also, let's define $\Psi(k)$ as

$$\Psi(k) := \text{“}\eta - (k-1) - C_k \sum_{i=k}^{N} {C_i}^{-1} > 0\text{”}. \tag{56}$$

Its negation will be denoted $\overline{\Psi(k)}$.

Consider $p \geqslant 1$ capacitors in parallel at cycle $n_p > n_0$, and $\Omega(p)$ is fulfilled. As (55) guarantees series switching at all cycles, and similarly to the case $\eta > N$ [see (35)]

$$\begin{aligned} \exists n_{p+1} \in \mathbb{N} \cup \{+\infty\}, n_{p+1} > n_p, I_p := [\![n_p; n_{p+1}[\![\\ \forall\, n \in I_p \qquad \tilde{\mathbf{V}}_{\overline{\mathbf{n}}} = (\tilde{\mathbf{A}}_{\mathbf{p}})^n\, \tilde{\mathbf{V}}_{\overline{\mathbf{0}}_{\mathbf{p}}} \\ \tilde{\mathbf{V}}_{\overline{\mathbf{0}}_{\mathbf{p}}} = \tilde{\mathbf{V}}_{\overline{\mathbf{n_p - 1}}} \end{aligned} \tag{57}$$

i.e., the evolution laws derived in Section IV-A given in (39) can be used in this interval.

1) Case $r_p > 1$: In this case, the conclusion is the same as in the $r_p > 1$ case of the analysis for $\eta > N$, in Section IV-A. A refinement of the latter case has to be used to infer conclusions in the summary: if $\Omega(p+1)$ in addition of $r_p > 1$, then $r_{p+1} > 1$.

2) Case $r_p < 1$: By virtually fixing the law (57)

$$\lim_{n \to +\infty} V_{\mathrm{var},\overline{n}} = \beta_{\mathrm{var},p}, \text{ and } \lim_{n \to +\infty} V_{p+1,\overline{n}} = \beta_{p+1,p}. \tag{58}$$

Also, some algebra yields

$$\forall\, i, p \in [[1; N]],\ \beta_{\mathrm{var},p} < \beta_{p+1,p} \Leftrightarrow \Psi(p+1). \tag{59}$$

Thus, if $\overline{\Psi(p+1)}$, then $n_{p+1} = +\infty$ and the voltages saturate following (58). Otherwise, $n_{p+1} < +\infty$, and $\Omega(p+1)$ holds, as it is implied by $r_p < 1$ and $\Psi(p+1)$.

3) Summary: As for the case $\eta > N$ in Section IV-A, inductively, the steady-state regime of the circuit can be characterized. As $\Psi(p+1) \Rightarrow \Psi(p)$, if there exists $p \in]\!]1; \lfloor \eta^- \rfloor]\!]$ such that $r_p > 1$, and $\Psi(p)$ is verified ($\lfloor \eta^- \rfloor = \eta - 1$ if $\eta \in \mathbb{N}$, $\lfloor \eta \rfloor$ otherwise), then the steady-state mode is an exponential mode. It is described as for the case $\eta > N$ (see the summary in Section IV-A4), with the following expression Π:

$$\Pi := \min\left(\left\{t \in [\![p; \lfloor \eta^- \rfloor]\!] |\ \overline{\Omega(t+1)}\right\}\right) \tag{60}$$

In particular, if operating in the exponential mode, the ratio between the transducer's extreme voltages across one cycle of operation is given by (52), with the parameter Π computed from (60).

Otherwise, if $r_p < 1$ for all p, or if $\overline{\Psi(p)}$ holds for all p, then the steady-state mode is a saturation regime,

Remark: This analysis refines the case $\eta > N$, as $\eta > N \Rightarrow$, $\forall\, p, \Psi(p)$.

Example (Bennet's Doubler): Let's investigate the particular case of the Bennet's doubler ($N = 2$), when $\eta \leqslant 2$, with $V_{\mathrm{var},\overline{n_0}} = V_{1,\overline{n_0}} > V_{2,\overline{n_0}}$, and supposing that (55) is fulfilled. As $r_1 < 1$, $\lim_{n \to +\infty} V_{2,\overline{n}} = \beta_{2,1}$. Defining σ as

$$\sigma := \frac{V_{\mathrm{var},\overline{n_0}}(\eta - 1)}{V_{\mathrm{var},\overline{n_0}}(\eta - 1) - V_{2,\overline{n_0}}} \tag{61}$$

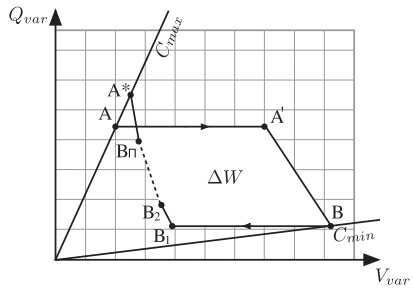

Fig. 4. The QV-cycle, for the generic circuit topology depicted in Fig. 3, as derived in Section V-A.

if $\sigma < 1 + r_1$, then an optimal cycle of index $n_{\mathrm{opt}} > n_0$ exists

$$n_{\mathrm{opt}_0} = n_0 + \left\lfloor \frac{\log(\sigma) - \log(1 + r_1)}{\log(r_1)} \right\rfloor. \tag{62}$$

Otherwise, $n_{\mathrm{opt}_0} = n_0$. These are simply found by solving for n the equation $\partial \Delta W_n / \partial n = 0$ with ΔW_n computed as in (53).

Note that the transient process leading to the exponential steady-state mode of the Bennet's doubler circuit, when $\eta > 2$, can be characterized in a similar way to this example.

V. Practical Considerations for Kinetic Energy Harvesting

A. Derivation of the Rectangular QV-Cycle

As stated in the introduction and Section II, the QV-cycle diagram is an intuitive geometrical tool that has been extensively used to describe the electrical operation of e-KEHs. It gives a clear view of the evolution of the transducer's biasing, and allows a quick estimation of the amount of converted energy during a cycle using simple geometric arguments: the converted energy in a given cycle is equal to the area enclosed by the QV loop for this cycle.

In the present subsection, the QV-cycle implemented by the circuits using the topology in Fig. 3 is sketched. The approximations that allow the diagram to be assimilated to the rectangular QV-cycle depicted in Fig. 2 are also discussed.

The derivation of the QV-cycle in this section is made under the condition $\eta > N$ (or $\eta \leqslant N$ in an exponential steady-state regime), for an arbitrary cycle of the steady-state mode of operation which was defined in Section IV-A4. Note that the derivation is made of for $V_{\mathrm{var},\overline{n}}/V_{i,\overline{n}}$ considered equal to the limit $(\Pi - 1)C_i/(C_{\max} + \sum_{i=1}^{\Pi} C_i))$, for $i \in]\!]\Pi; N]\!]$. The constant Π is defined as in (51).

1) Exact Derivation: Starting from the point A (see Fig. 4), with C_{var} decreasing from $C_{\mathrm{var}} = C_{\max}$, no current is flowing, and V_{var} increases as stated in (4), hence the horizontal segment [AA'] in the QV plane.

When, at each cycle, $V_{\mathrm{var}}(t)$ reaches the sum of the voltages across all the fixed capacitors, a current flows and the variation law of V_{var} changes accordingly to (10). The equation of the corresponding segment [A'B] in the QV plane is given by:

$$\begin{aligned} Q_{\mathrm{var}}(t) = -V_{\mathrm{var}}(t) \left(\sum_{i=1}^{N} {C_i}^{-1}\right)^{-1} + \left(\sum_{i=1}^{N} {C_i}^{-1}\right)^{-1} \\ \times \left(\Pi + \frac{C_{\max} + \sum_{i=1}^{k} C_i}{\Pi - 1} \sum_{i=\Pi+1}^{N} {C_i}^{-1}\right) V_{\mathrm{var},\overline{n}}. \end{aligned} \tag{63}$$

Now, starting from the point B, with $C_{\rm var}$ increasing from $C_{\min}$, no current is flowing, and $V_{\rm var}$ decreases as stated in (16), hence the horizontal segment $[{\rm BB}_1]$ in the QV plane.

When, at each cycle, $V_{\rm var}(t)$ reaches the voltage of the smallest capacitor, a current flows and the law of variation of $V_{\rm var}$ changes, as given in (19). This repeatedly occurs with the other fixed capacitors, until $C_{\rm var} = C_{\max}$.

The equations of the corresponding segments $[B_jB_{j+1}]$ in the QV plane are given by, with $j \in [\![1; k[\![$

$$Q_{{\rm var}_j}(t) = -V_{\rm var}(t)\sum_{i=1}^{j} C_i + V_{{\rm var},\overline{n}} \times \left[C_{\max} + \sum_{i=1}^{j} C_i + \left(j-1\right) \times \left(C_{\max} - C_{\min}\left(\Pi + \frac{C_{\max} + \sum_{i=1}^{k} C_i}{\Pi - 1} \sum_{i=\Pi+1}^{N} {C_i}^{-1}\right)\right)\right] \tag{64}$$

When $C_{\rm var} = C_{\max}$ at the cycle $n+1$, the voltage and charge coordinates of the point have increased compared to $C_{\rm var} = C_{\max}$ at the cycle n ($V_{{\rm var},\overline{n+1}} = r_\Pi V_{{\rm var},\overline{n}},\ r_\Pi > 1$).

2) Approximation to a Rectangular QV-Cycle: The equation (63) shows that if $C_{\min} < C_{\max} \ll \min_{1 \leqslant i \leqslant N} C_i$, then the segment [A'B] can be considered as vertical going through A'. Also, under the same condition, equation (64) allows the segment [BA*] to be considered vertical, and going through $A^* = A$ as $r_\Pi \approx 1^+$.

In light of these considerations, when $C_{\max}$ is sufficiently small compared to the values of the fixed capacitors, the cycle can be approximated by the ideal rectangular QV-cycle depicted in Fig. 2. The parameter q of the ideal rectangular QV-cycle (see Fig. 2) is expressed as

$$q = \Pi + \frac{C_{\max} + \sum_{i=1}^{\Pi} C_i}{\Pi - 1} \sum_{i=\Pi+1}^{N} {C_i}^{-1}. \tag{65}$$

This can also be seen algebraically by simplifying (52) with $C_{\max}$, $C_{\min}$ small compared to the C_i's.

The harvested energy per cycle in the steady-state exponential mode can then be approximated by the area of the obtained rectangle

$$\Delta W_n = C_{\min} {V_{{\rm var},\overline{n}}}^2 (q-1)(\eta - q). \tag{66}$$

B. Possible Uses of the Proposed Conditioning

1) Electrical Domain: Some possible advantages of conditioning circuits with exponential regimes over other charge-pump conditioning circuits for e-KEH have already been discussed in the introduction and, for example, in [9] and [11]. However, the comparison depends on the application context, defined by the input and the constraints on the system. In the following, an example of a situation is presented, for which it is advantageous to use a circuit showing an exponential regime in which the transducer is biased by extreme voltages of ratio greater than 2 at each cycle.

The application context is the following: suppose there exists a maximal allowable voltage V_M across the transducer, $\eta > N$,

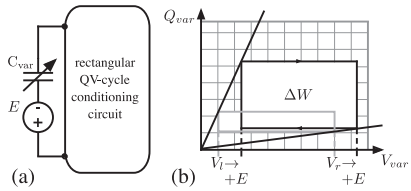

Fig. 5. (a) Electrical model for an electret-charged transducer (b) The effect of the electret on a rectangular QV-cycle.

and the transducer is supposed to use of electret charging to provide a built-in polarization of the transducer (see for example [12], [13]), with no external pre-charging of the circuit's fixed capacitors. This built-in bias also provides an initial voltage to e-KEHs using a conditioning circuit with exponential voltage increasing regime, as has been experimentally verified in [14]. A simple electrical model of the electret-charged transducer is represented in Fig. 5(a). The conditioning circuit hence biases the dipole $\{\text{transducer} + \text{electret}\}$, rather than directly the transducer. The effect of the electret on the conditioning scheme is summarized by a voltage offset of E, the value of the electret's model equivalent voltage source. This is visible on the QV-cycle depicted in Fig. 5(b).

In [4], the optimal rectangular QV-cycle conditioning scheme was derived as a function of η, under the constraint of a fixed maximal voltage V_M. The optimal cycle was shown to be obtained with the following optimal biasing: the upper transducer bias voltage is fixed to V_M, and the ratio between the upper and lower voltages biasing the transducer across one period of the external vibration is:

$$q_{\text{opt transducer}} = \frac{2\eta}{\eta + 1}. \tag{67}$$

In these conditions, to achieve the ratio in (67) between the upper and lower biasing voltages of transducer across the transducer, using an electret, one has to use a circuit with the ratio

$$q_{\text{opt transducer+elec}} = \frac{2\eta(V_M - E)}{V_M(\eta + 1) - 2E\eta} \tag{68}$$

between the extreme voltages biasing the dipole $\{\text{transducer} + \text{electret}\}$ throughout each cycle. The ratio in (68) can be greater than 2. A circuit derived from the topology proposed in this paper, with an appropriate choice of the capacitors, can implement this biasing scheme. To do so, the fixed capacitors values have to be chosen so to equate (65) with (68) (reminding that Π depends on the fixed capacitors values, as derived in Section IV-A4 and B3). An external interface has to let the circuit reach the optimal cycle and then sustain it, as will be discussed in Section V-D.

Note that in the example presented above, the use of a saturating charge-pump conditioning circuit (e.g., the simple rectifier circuits presented in [13], that are widely used with electret e-VEHs) instead of the proposed circuit can only be comparatively disadvantageous. Indeed, the absolute maximal harvested power would intrinsically be limited by E and η, because of the saturation phenomenon. This would lead to an inferior or equal maximal harvested power, compared to the circuit discussed above, which does not exhibit saturation. For the exponential conversion mode circuit, a maximal harvested power only exists because of the maximal voltage constraint,

provided that η is such that the circuit is in its steady-state exponential regime.

2) Complete System's Dynamics: Electro-Mechanically-Coupled Case: Note that in real e-KEHs, the electromechanical coupling drastically impacts the dynamics of the whole system ($\{\text{electrical} + \text{mechanical}\}$), whereas in the present study, C_{var} has been considered as an unalterable input. In light of these considerations, it is necessary to adjunct the present study to semi-analytical tools, simulation, and/or measurements to accurately describe the coupled e-KEH's dynamics, so as to guide design choices and optimization for a given application context. For example, the work in [15] analyzes the coupled behavior of an e-KEH using a generic conditioning circuit of the charge-pump family, under fixed harmonic vibration input excitation of the mechanical system. Particularly, the dependence of the system's dynamics to the exact shape of the rectangular QV-cycle was highlighted. As examples have recently shown that exponential mode conditioning circuits often give better energy conversion figures than other conditioning circuits [14], it is of great interest to build a toolbox of conditioning circuits with different extreme bias ratio at the scale of one cycle (i.e., QV-cycle aspect ratios), that do not saturate in large time scale of autonomous operation in the electrical domain. It gives the designer a wider choice of conditioning schemes to fulfill the optimal conditioning determined by the coupled system's study. The generic topology presented in this paper adds to this range of available conditioning circuits.

C. Effect of the Electrical Nonidealities

The analysis carried out in Sections III and IV does not include parasitic effects of the electrical components. In particular, the diodes are considered ideal, i.e., zero-current for reverse bias and ideal zero-voltage source for forward bias, with zero threshold voltage. These nonidealities have an impact on the circuit dynamics. However, these effects are of higher order, and do not qualitatively change the results of the analysis carried out in the rest of the paper. In this subsection, the effect of different nonidealities of the circuit's electrical components are qualitatively discussed.

1) Non-Null Diodes Forward Voltage Drop: Considering an ideal diode model with a non-null forward voltage drop has an effect on the explicit voltages evolution over time [this can be seen in the simulations results, Section V-E, by comparing Fig. 8(b) and (c)]. Interestingly, it is worth noting that introducing this nonideality does not change the obtained conditions and extreme transducer biasing ratios for the different operation modes. A proof of that fact and the modified evolution laws can be found analytically by changing the local evolution laws of Section III, so to take in account a constant threshold V_T. The rest of the analysis is very similar to what is done in Sections III and IV. The coefficient in r_p in (38) is not altered, but the expressions for coefficients $\alpha_{i,j}$ and $\beta_{i,j}$ in (42)–(45) are affected. However, their expressions become heavier and uncomfortable to work with to derive the steady-state characteristics as done in Section IV. The fact that r_p is not modified implies that for large time scales in the steady-state mode, the ratio between the explicit evolution laws with and without taking in account a constant threshold voltage is constant. Note that in practice, taking in account this nonideality suffices to give very accurate results on the explicit long term dynamics, provided that V_T is chosen accordingly to the average currents that flow through the diodes.

2) Diodes' Reverse Parasitic Capacitance: The diodes' reverse capacitances are responsible for a small change of the conditions for the different operation modes. Again, it is possible to quantify this effect by rewriting the laws in Section III so to take in account the charge exchange between the transducer and the diodes' capacitances, when the transducer's capacitance is varying. However, this results in mathematically cumbersome evolution laws. Still, this effect can be estimated by a modification of the QV-cycle derived in Section V-A. To do so, it suffices to turn the horizontal segments into segments with a negative slope, whose value is dictated by the value of the equivalent capacitance seen by the transducer, when the diodes are not conducting [see simulation result in Fig. 8(f)]. In practical cases, the transducer's capacitance is such that this effect is negligible. For example, JPAD5 didoes have a 2 pF reverse capacitance value for a wide voltage range. The induced negative slope in the QV-cycle is negligible provided that the transducer's capacitance values are typically an order of magnitude above.

3) Reverse Currents, Capacitors Leakages: Other nonidealities include the capacitors leakages and the diodes reverse currents. If the diodes' breakdown voltage is not reached, these leakages are usually so low that their effect on the circuit's dynamics is negligible. However, they can become important at high time scales during which the system is not submitted to input excitations.

It is worthy to note that in practical e-VEHs, the effect of the electromechanical coupling on the dynamics derived in the present work is undoubtedly prominent over the modifications of the evolution laws consecutive to the circuit's nonidealities.

D. Energy Extraction and Load Interface

The energy converted by an e-KEH is first stored in the reactive elements of the conditioning circuit. Because of the constraints on the form of the energy needed by the load (e.g., load voltage requirements), an intermediary interface circuit is needed between the conditioning circuit and the load. This interface circuit has to (i) extract the energy from the conditioning circuit and (ii) deliver it in a suitable form to the load (e.g., load's nominal voltage requirement).

The task (i) is equivalent to controlling the rate at which energy is extracted from the conditioning circuit, eventually knowing the rate at which it is converted. As a result, at least a part of the intermediary interface circuit has a direct influence on the operation of the conditioning circuit. The circuit depicted in Fig. 6 is a simple candidate to fulfill the task (i) for e-KEHs using the conditioning circuits reported in this paper. The same principles can apply to a wide range of conditioning circuits for e-KEH. The task (ii) is relatively independent of the used conditioning circuit, and will not be discussed here. These tasks have to be done whilst ensuring that the conditioning circuit biases the transducer in an optimal way, in the various context-dependent senses, e.g., the situation discussed in Section V-B. Few examples of such situation are now discussed.

For example, suppose N fixed, $\eta > N$, and the electromechanical coupling is neglected. If the only constraint is a fixed maximal voltage V_M across the transducer, the voltage

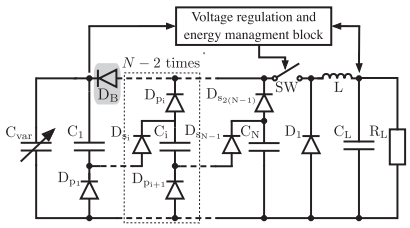

Fig. 6. The generic circuit with an energy extracting interface.

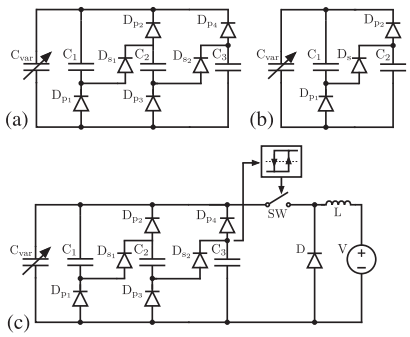

Fig. 7. (a) Simulated circuit, corresponding to the generic topology in Fig. 3, with $N = 3$. (b) Simulated circuit, corresponding to the generic topology in Fig. 3, with $N = 2$ (Bennet's doubler). (c) The circuit simulated with an implementation of the energy extracting interface.

regulation block has to discharge the conditioning circuit ensuring that the upper extreme voltage across the transducer stays as close as possible to $V_M{}^-$. For a given rectangular QV-cycle, to this upper voltage corresponds the maximal converted energy per cycle. This can be done, for example, by sensing the value of the voltage across one of the fixed capacitors, and discharging the circuit's fixed capacitors by closing the switch when the voltage exceeds a given value $V_{\text{comp}} + V_h < V_M$, and opening the switch when the voltages falls below a given value $V_{\text{comp}} - V_h$ (comparison with hysteresis). The choice of (V_{comp}, V_h) depends on the application context (e.g., requirement on the frequency of recharging of the output capacitor). See Fig. 8(i) for a simulation of this example.

As an other example, let's consider an application where the system is to operate often with $\eta \leqslant N$. In this case, it may be interesting to add the diode D_B depicted in Fig. 6. Starting from a case where all the capacitors have the same voltage, evenly discharging all of the capacitors (no diode D_B) results in the condition (55) not to be fulfilled, hence leading to no energy conversion process. By adding the diode D_B, the capacitor C_1 is not discharged by the voltage regulation block. Choosing this capacitor to be the smallest among circuit's fixed capacitors minimizes the amount of converted energy that will not be delivered to the load. In these conditions, the voltage regulation block has to discharge the conditioning circuit so as to stay as close as possible of the optimal voltage for the case $\eta \leqslant N$.

Finally, an important situation is the existence of an optimal voltage consecutive to the effect of the electromechanical coupling. The proposed interface can also be used to stay at this optimal point of power conversion in this case.

E. Simulations

In this section, results of simulations carried out with Linear Technology's LTSpice IV and Mentor Graphic's Eldo [for the simulation in Fig. 8(c) and (f)] are given, to support the conditions for the different operation regimes of the circuit and the extreme biasing ratios, all given in Section IV-A4 and B3. In this view, the proposed topology is simulated with $N = 3$ [see Fig. 7(a)] for the exponential mode, and with $N = 2$ [see Fig. 1(c), without considering the current source] for an example of saturating mode of the Bennet's doubler. The transducer's variable capacitance C_{var} was chosen varying sinusoidally with a frequency of 100 Hz.

For the simulation in Fig. 8(a), the parameters were chosen such that $\Omega(3)$ is fulfilled, and thus, the circuit enters a steady-state mode during which all the capacitors of the network are in parallel at $C_{\text{var}} = C_{\max}$. The exact values of the parameters are: $C_{\min} = 25$ pF, $C_{\max} = 175$ pF, $C_1 = 1$ nF, $C_2 = 10$ nF and $C_3 = 11$ nF. The initial voltages are $V_{\text{var},\overline{0}} = V_{1,\overline{0}} = 5$ V, $V_{2,\overline{0}} = V_{3,\overline{0}} = 0$ V.

For the simulation in Fig. 8(b), the parameters were chosen such that $\Omega(3)$ is not fulfilled. The steady-state mode of operation begins at the time which is zoomed in the figure. At every cycle in this mode of operation, C_1 and C_2 are in parallel at $C_{\text{var}} = C_{\max}$. The voltage across C_3 is lower, and C_3 is never in parallel with C_1 and C_2 in the steady-state. The exact values of the parameters are: $C_{\min} = 25$ pF, $C_{\max} = 175$ pF, $C_1 = 1$ nF, $C_2 = 10$ nF and $C_3 = 20$ nF. The initial voltages are $V_{\text{var},\overline{0}} = V_{3,\overline{0}} = 5$ V, $V_{1,\overline{0}} = V_{2,\overline{0}} = 0$ V.

On the QV-cycles for both simulations, depicted in Fig. 8(d) and (e), the ratios of the extreme voltages across the transducer are given. The value of these ratios correspond to the analytical ratio predicted in (52). As $C_{\max}$ was not chosen much smaller than C_1, the QV-cycles are closer to the general shape of Fig. 4.

In Fig. 8(c), the results of the same simulation as in Fig. 8(b) are depicted, using a more accurate model of the diodes. The used model is an exponential level 1 model, with default Spice parameter values (saturation current of 1 pA), and a parasitic capacitance of 2 pF (corresponding for example to the JPAD5 diode capacitance). Note that although the long term voltage evolution is quantitatively different compared to Fig. 8(b), locally, the QV-cycle is almost unaltered: the extreme voltage biasing ratio of the capacitor is not changed. The effect of the diodes' parasitic capacitances is visible by the slight modification of the slopes of the segments of the QV-cycle. The deviation from the result in Fig. 8(c) can be almost totally predicted, by using the ideal diode model with constant voltage threshold, discussed in Section V-C1: the other nonidealities (parasitic capacitance and use of an exponential diode model instead of an ideal diode model) are of much higher order and do not change the results qualitatively and quantitatively.

The simulation results in Fig. 8(g) and (h) show examples of the circuit working with $\eta \leqslant N$. In Fig. 8(g), an example of an exponential operation regime with $\eta \leqslant N = 3$ is shown, illustrating what was discussed in the end of Section IV-B, as $r_2 > 1$. The exact values of the parameters are: $C_{\min} = 60$ pF, $C_{\max} = 140$ pF, $C_1 = 1$ nF, $C_2 = 5$ nF and $C_3 = 25$ nF. The initial voltages are $V_{\text{var},\overline{0}} = V_{1,\overline{0}} = 5$ V, $V_{2,\overline{0}} = V_{3,\overline{0}} = 0$ V.

In Fig. 8(h), the case $N = 2$ is simulated (Bennet's doubler). A maximal power point (inflexion point on the energy over time graph) is highlighted. This point exists accordingly to the discussion in Section IV-B. The initial conditions are chosen such that the cycle n for this maximal power point is strictly positive (0 being the cycle at $t = 0$). The exact value of the

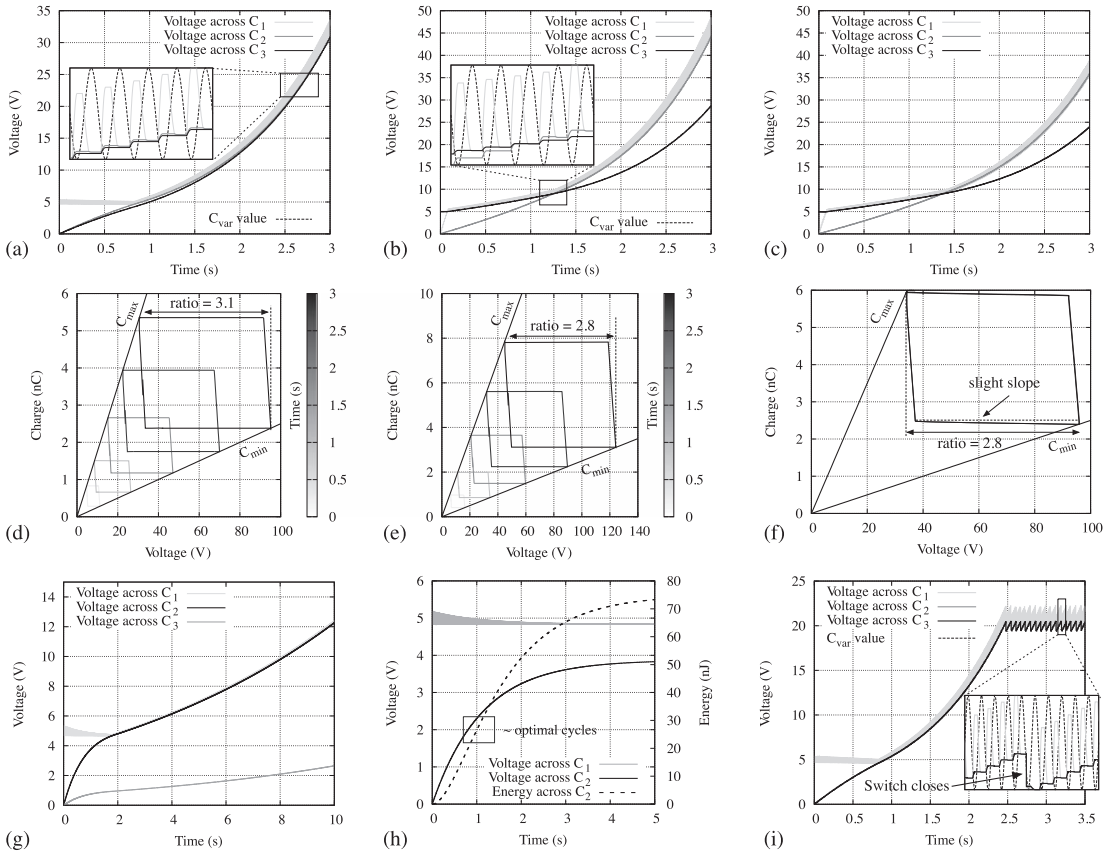

Fig. 8. Simulation results: (a) voltages evolution for the circuit depicted in Fig. 7(a), $\eta > N$, $\Omega(3)$ is fulfilled. (b) voltages evolution for the circuit depicted in Fig. 7(a), $\eta > N$, $\Omega(3)$ is not fulfilled. (c) voltages evolution for the same simulation as in (a), with exponential diode model. (d) QV-cycle corresponding to the evolution depicted in (a), plotted at different instants. (e) QV-cycle corresponding to the evolution depicted in (b), plotted at different instants. (f) QV-cycle corresponding to the evolution depicted in (c), plotted at one instant. (g) voltages evolution for the circuit depicted in Fig. 7(a), $\eta < N$, with exponential steady-state regime. (h) voltages and energy evolution for the circuit in Fig. 7(b) (Bennet's doubler), $\eta < N$, showing an optimal power point. (i) voltages evolution for the circuit depicted in Fig. 7(c) (with an energy extracting interface).

parameters are: $C_{\min} = 100$ pF, $C_{\max} = 180$ pF, $C_1 = 1$ nF and $C_2 = 10$ nF. The initial voltages are $V_{\text{var},\overline{0}} = V_{1,\overline{0}} = 5$ V, $V_{2,\overline{0}} = 0$ V.

The time evolutions of the voltages in Fig. 8(a), (b), (g), and (h) were checked against the explicit evolution laws, following the considerations of the remark in the end of Section IV-A4, and match perfectly with the theory. To simplify the verification of the derived dynamics, the reader who does not want to spend time building the explicit evolution laws including the transient evolution can apply the evolution laws of the steady-state definition region directly, choosing the initial voltages as the voltages at the time when the steady-state mode is entered. This is the voltages at $t \approx 2.5$ s for Fig. 8(a), $t \approx 1.25$ s for Fig. 8(b), $t \approx 1.8$ s for Fig. 8(g) and $t = 0$ s for Fig. 8(h).

Finally, Fig. 8(i) gives the result of the simulation of the circuit in Fig. 7(b), i.e., the same circuit connected to a load interface based on the one presented in Section VI. The switch control is as described in the first example situation discussed in Section V-D, sensing the voltage across C_3, with $V_{\text{comp}} = 20$ V and $V_h = 0.5$ V. To discard any consideration about the regulation of voltage on the output capacitor (task (ii) in Section V-D), the output capacitor is modeled as a voltage source of 5 V. This can also model a practical case, where the output capacitor is replaced by a battery. The simulation is carried out with $C_{\min} = 25$ pF, $C_{\max} = 175$ pF, $C_1 = 1$ nF, $C_2 = 10$ nF, $C_3 = 10$ nF, and $L = 100$ μH.

VI. Conclusion

This work presented a new generic circuit topology to implement series-parallel charge pumps driven by a variable capacitor, that can be used as an e-KEH's conditioning circuits. A throughout analysis was carried out so to give a formal and rigorous derivation of the circuit's dynamics. From a practical energy harvesting application point of view, insights about the dynamics and design of the system including an energy extracting interface were given.

The circuits derived from this generic topology show exponential steady-state modes during which is implemented, at each cycle of the capacitance variation, a biasing scheme of the transducer described by a rectangular QV diagram with any extreme voltage ratios greater than 2. This ratio is can be set by the choice of the circuit's components. With the original Bennet's doubler and its previously-reported extensions, only fixed rational ratios of the form $(N+1)/N$, where N is a non-null integer, were possible. Hence, the proposed topology successfully complements the existing set of the conditioning circuits inspired from the Bennet's doubler architecture.

The non-exponential steady-state mode was also analyzed, in the case of low capacitance variation value. This analysis also holds for the Bennet's doubler, for which the dynamics of this mode were not described so far.

An example for which the reported topology is advantageous over state-of-the art circuits has been given. However, this example is limited to an electrical domain study. To be able to advocate for a particular conditioning aiming for design and optimization, an electromechanical study is required to predict the full e-KEH's dynamics. Apart from experimental and numerical simulation methods, applying semi-analytical tools that were developed (e.g., in [15]) are a mean to assess such a study. Applying these tools requires a comprehension of the conditioning circuit's dynamics, as provided by this paper.

APPENDIX
PROOF OF THE LEMMA USED IN SECTION IV

Consider two fixed capacitors of the network, C_1 and C_2. Let

$$\mathcal{Q}_i^j = \{n \in \mathbb{N} \mid n \geqslant i, V_{\mathrm{var},\overline{n}} = V_{j,\overline{n}}\}$$
$$\mathcal{S}_i^j = \left\{n \in \mathbb{N} \mid n \geqslant i, (V_{\mathrm{var},\overline{n-1}} = V_{j,\overline{n-1}}) \wedge (V_{\mathrm{var},\overline{n}} \neq V_{j,\overline{n}})\right\}.$$

(a) Consider a cycle n_1 such that $\mathcal{Q}_{n_1}^1 \cup \mathcal{Q}_{n_1}^2 = \emptyset$. In this case, the evolution laws derived in Section III lead to (evolution with no parallel configuration of C_1 and/or C_2 with C_{var}). As at each cycle, the switching in series will necessarily occur, since $\eta > N$

$$\forall\, n \geqslant n_1, \quad \begin{aligned} V_{1,\overline{n}} &= V_{1,\overline{n_1}} + \tfrac{1}{C_1} \sum_{k=n_1}^{n} \Delta Q_k \\ V_{2,\overline{n}} &= V_{2,\overline{n_1}} + \tfrac{1}{C_2} \sum_{k=n_1}^{n} \Delta Q_k \end{aligned} \tag{69}$$

with ΔQ_k defined in (13). Thus

$$\begin{aligned} \forall\, n \geqslant n_1,\ \Delta_n &= V_{1,\overline{n}} - V_{2,\overline{n}} \\ &= V_{1,\overline{n_1}} - V_{2,\overline{n_1}} + \frac{C_2 - C_1}{C_1 C_2} \sum_{k=n_1}^{n} \Delta Q_k \end{aligned} \tag{70}$$

where

$$\sum_{k=n_1}^{n} \Delta Q_k = \sum_{k=n_1}^{n} \left(\frac{C_{\min}}{1 + C_{\min} \sum_{i=1}^{N} {C_i}^{-1}} \times \left(V_{\mathrm{var},\overline{k}}(\eta - p_k) - \sum_{i=p_k+1}^{N} V_{i,\overline{k}} \right) \right) \tag{71}$$

and where p_k is the number of capacitors in parallel with C_{var} in cycle k at $C_{\mathrm{var}} = C_{\max}$. Hence, since for any $(k,i) \in \mathbb{N} \times [\![1; N]\!]$, $V_{i,\overline{k}} \leqslant V_{\mathrm{var},\overline{k}}$, and under the condition $\eta > N$

$$\begin{aligned} &\frac{C_{\min}}{1 + C_{\min} \sum_{i=1}^{N} {C_i}^{-1}} \left(V_{\mathrm{var},\overline{k}}(\eta - p_k) - \sum_{i=k_i+1}^{N} V_{i,\overline{k}} \right) \\ &\qquad \geqslant C_{\min} \frac{V_{\mathrm{var},\overline{n_1}}(\eta - N)}{1 + C_{\min} \sum_{i=1}^{N} {C_i}^{-1}} > 0. \end{aligned} \tag{72}$$

Therefore, the sequence $(\Delta_n)_{n \geqslant n_1}$ diverges to $+\infty$ if and only if $C_1 < C_2$, to $-\infty$ if and only if $C_2 < C_1$. Consequently, eventually swapping the capacitors indexes in the case $C_1 = C_2$ so as to have $V_{1,\overline{n_1}} \geqslant V_{2,\overline{n_1}}$

$$\exists n_1' \geqslant n_1,\ \forall\, n,\ n \geqslant n_1' \Rightarrow (V_{1,\overline{n}} \geqslant V_{2,\overline{n}} \Leftrightarrow C_1 \leqslant C_2). \tag{73}$$

(b) Consider a cycle $n_2(i)$ such that $\mathcal{Q}_{n_2(i)}^1 \cup \mathcal{Q}_{n_2(i)}^2 \neq \emptyset$. Suppose $V_{1,\overline{n_2(i)}} \geqslant V_{2,\overline{n_2(i)}}$.

(b.1) First, the case when $C_1 \leqslant C_2$ is investigated. From (69), with $n_1 = n_2(i)$, it follows that $\mathcal{Q}_{n_2(i)}^1 \neq \emptyset$ and:

$$C_1 \leqslant C_2 \Rightarrow \left(\forall\, n \in [\![n_2(i); \min \mathcal{Q}_{n_2(i)}^1 [\![,\ V_{1,\overline{n}} \geqslant V_{2,\overline{n}} \right). \tag{74}$$

(b.1.1) If $\mathcal{S}_{n_2(i)}^1 = \emptyset$, (74) can be extended to any cycle after $n_2(i)$

$$C_1 \leqslant C_2 \Rightarrow (\forall\, n, n \geqslant n_2(i) \Rightarrow V_{1,\overline{n}} \geqslant V_{2,\overline{n}}). \tag{75}$$

(b.1.2) Now, suppose $\mathcal{S}_{n_2(i)}^1 \neq \emptyset$.

(b.1.2.1) On the one hand, note that

$$\forall\, n \in [\![\min \mathcal{Q}_{n_2(i)}^1; \min \mathcal{S}_{n_2(i)}^1 [\![,\ V_{1,\overline{n}} \geqslant V_{2,\overline{n}}. \tag{76}$$

(b.1.2.2) On the other hand, [see condition (17)]

$$\forall\, n \in \mathcal{S}_{n_2(i)}, \qquad V_{1,\underline{n}} < V_{\mathrm{var},\overline{n}} \tag{77}$$

with, from (12), and with ΔQ_n defined in (13)

$$\begin{aligned} \forall\, n,\ V_{1,\overline{n}} &= V_{1,\overline{n-1}} + \frac{\Delta Q_{n-1}}{C_1} \\ \forall\, n,\ V_{2,\overline{n}} &= V_{2,\overline{n-1}} + \frac{\Delta Q_{n-1}}{C_2}. \end{aligned} \tag{78}$$

Hence

$$\begin{aligned} &\left((C_1 \leqslant C_2) \wedge \left(\forall\, k \in \mathcal{S}_{n_2(i)},\ V_{1,\overline{k-1}} \geqslant V_{2,\overline{k-1}} \right) \right) \\ &\quad \Rightarrow \forall\, n \in \mathcal{S}_{n_2(i)},\ V_{2,\underline{n}} \leqslant V_{1,\underline{n}} < V_{\mathrm{var},\overline{n}} \\ &\quad \Rightarrow \forall\, n \in \mathcal{S}_{n_2(i)},\ V_{2,\overline{n}} = V_{2,\underline{n}} \leqslant V_{1,\overline{n}} = V_{1,\underline{n}}. \end{aligned} \tag{79}$$

Putting it all together, from (74) and (75) comes

$$C_1 \leqslant C_2 \Rightarrow \left(\forall\, n \in [\![n_2(i); \min \mathcal{S}_{n_2(i)}^1 [\![,\ V_{1,\overline{n}} \geqslant V_{2,\overline{n}} \right) \tag{80}$$

and from (79), the above reasoning starting from ***(b.1)*** can then be inductively repeated choosing $n_2(i+1) = \min \mathcal{S}_{n_2(i)}^1$: if $\mathcal{Q}_{n_2(i)}^1 \cup \mathcal{Q}_{n_2(i)}^2$ is not a finite set, then inductively

$$C_1 \leqslant C_2 \Rightarrow (\forall\, n,\ n \geqslant n_2 \Rightarrow V_{1,\overline{n}} \geqslant V_{2,\overline{n}}). \tag{81}$$

Otherwise, if there exists $n_2(j) \in \mathcal{S}_{n_2(j-1)}^1$ such that $\mathcal{Q}_{n_2(j)}^1 \cup \mathcal{Q}_{n_2(j)}^2 = \emptyset$, then ***(a)*** can be applied, choosing $n_1 = n_2(j)$, and the same conclusion, i.e., (81), holds.

(b.2) Consider now $C_2 < C_1$. Let $\mathcal{T}_i^{a,b}$ be the set such that:

$$\mathcal{T}_i^{a,b} = \{n \in \mathbb{N} \mid (V_{a,\overline{n}} \geqslant V_{b,\overline{n}}) \wedge (n \geqslant i)\}.$$

Suppose $\mathcal{T}^{2,1}_{n_2(i)} = \emptyset$. Then, the laws of variation of voltages on both capacitors are

$$\forall\, n \geqslant n_2(i), \quad \begin{aligned} V_{1,\overline{n}} &= V_{1,\overline{n_2(i)}} + \tfrac{1}{C_1} \sum_{k=n_2(i)}^{n} \Delta Q_k - \Delta V_n \\ V_{2,\overline{n}} &= V_{2,\overline{n_2(i)}} + \tfrac{1}{C_2} \sum_{k=n_2(i)}^{n} \Delta Q_k \end{aligned} \tag{82}$$

where the term ΔV_n represents decrease of the voltage across C_1 when it is in parallel with $C_{\rm var}$. As, $\forall\, n$, $\Delta V_n \geqslant 0$, it comes, with (Δ_n) defined in (70)

$$V_{1,\overline{n}} - V_{2,\overline{n}} \leqslant \Delta_n \tag{83}$$

and as $C_2 < C_1$ implies that $(\Delta_n)_{n \geqslant n_2(i)}$ diverges to $-\infty$, $(V_{1,\overline{n}} - V_{2,\overline{n}})_{n \geqslant n_2(i)}$ diverges to $-\infty$, and hence a contradiction since it would therefore exist $n \geqslant n_2(i)$ such that $V_{1,\overline{n}} \leqslant V_{2,\overline{n}}$. Thus, $\mathcal{T}^{2,1}_{n_2(i)} \neq \emptyset$ and, applying ***(b.1)*** with initial cycle $n_2(j) = \min \mathcal{T}^{2,1}_{n_2(i)}$ and swapping the capacitors indexes, all the cases are covered. Applying the proof to every couple of fixed capacitors in the network, the implication part of the proof is concluded for the voltages at $C_{\rm var} = C_{\max}$. From (12) and the capacitance values order, it is clear that the conclusion also holds for $C_{\rm var} = C_{\min}$.

The proof of the converse, which is not useful in the application of the lemma, easily follows by *reductio ad absurdum*.

REFERENCES

[1] B. C. Yen and J. H. Lang, "A variable-capacitance vibration-to-electric energy harvester," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 2, pp. 288–295, 2006.

[2] A. Kempitiya, D.-A. Borca-Tasciuc, and M. M. Hella, "Analysis and optimization of asynchronously controlled electrostatic energy harvesters," *IEEE Trans. Ind. Electron.*, vol. 59, no. 1, pp. 456–463, 2012.

[3] S. Roundy, P. K. Wright, and J. Rabaey, "A study of low level vibrations as a power source for wireless sensor nodes," *Comput. Commun.*, vol. 26, no. 11, pp. 1131–1144, 2003.

[4] D. Galayko, A. Dudka, A. Karami, E. O'Riordan, E. Blokhina, O. Feely, and P. Basset, "Capacitive energy conversion with circuits implementing a rectangular charge-voltage cycle—Part 1: Analysis of the electrical domain," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 9, pp. 2652–2663, 2015.

[5] S. Meninger, J. O. Mur-Miranda, R. Amirtharajah, A. P. Chandrakasan, and J. H. Lang, "Vibration-to-electric energy conversion," *IEEE Trans. Very Large Scale Integr (VLSI) Syst.*, vol. 9, no. 1, pp. 64–76, 2001.

[6] P. Mitcheson, T. Sterken, C. He, M. Kiziroglou, E. Yeatman, and R. Puers, "Electrostatic microgenerators," *Meas. Control*, vol. 41, no. 4, pp. 114–119, 2008.

[7] A. C. M. de Queiroz and M. Domingues, "The doubler of electricity used as battery charger," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 58, no. 12, pp. 797–801, 2011.

[8] A. Bennet and R. Kaye, "An account of a doubler of electricity," *Philos. Trans. Roy. Soc. London*, vol. 77, pp. 288–296, 1787.

[9] E. Lefeuvre, S. Risquez, J. Wei, M. Woytasik, and F. Parrain, "Self-biased inductor-less interface circuit for electret-free electrostatic energy harvesters," in *J. Phys., Conf. Series*, vol. 557, 2014, p. 012052.

[10] J. Wei, S. Risquez, H. Mathias, E. Lefeuvre, and F. Costa, "Simple and efficient interface circuit for vibration electrostatic energy harvesters," in *Proc. IEEE SENSORS*, 2015, pp. 1–4.

[11] A. C. M. De Queiroz, "Electrostatic vibrational energy harvesting using a variation of Bennet's doubler," in *Proc. 53rd IEEE Int. Midwest Symp. Circuits Syst*, 2010, pp. 404–407.

[12] T. Sterken, P. Fiorini, K. Baert, R. Puers, and G. Borghs, "An electret-based electrostatic μ-generator," in *Proc. 12th Int. Conf. TRANSDUCERS, Solid-State Sensors, Actuators, Microsyst.*, vol. 2, 2003, pp. 1291–1294.

[13] Y. Suzuki, "Electret based vibration energy harvester for sensor network," in *Proc. 18th Int. Conf. Solid-State Sensors, Actuators, Microsystems (TRANSDUCERS)*, 2015, pp. 43–46.

[14] A. Karami, P. Basset, and D. Galayko, "Electrostatic vibration energy harvester using an electret-charged mems transducer with an unstable auto-synchronous conditioning circuit," *J. Phys., Conf. Series*, vol. 660, no. 1, p. 012025, 2015.

[15] E. O'Riordan, A. Dudka, D. Galayko, P. Basset, O. Feely, and E. Blokhina, "Capacitive energy conversion with circuits implementing a rectangular charge-voltage cycle part 2: Electromechanical and nonlinear analysis," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 11, pp. 2664–2673, 2015.

Armine Karami (S'14) was born in Paris, France, in 1991. He received the M.S. degree in electrical engineering from Université Pierre et Marie Curie—Paris 6, France, (UPMC) in 2014. He is currently working toward the Ph.D. degree in Université Pierre et Marie Curie (UPMC)—Paris 6, at the Laboratoire d'Informatique de Paris 6 (LIP6). His Ph.D. research is focused on the theory and analysis of electrostatic kinetic energy harvesting systems.

Dimitri Galayko (M'12) graduated from Odessa State Polytechnich University, Ukraine, in 1998, he received his M.S. degree from Institut of Applied Sciences of Lyon (INSA-LYON), France, in 1999. He made his Ph.D. thesis in the Institute of Microelectronics and Nanotechnologies (IEMN, Lille, France) and received the Ph.D. degree from the University Lille-I in 2002. The topic of his Ph.D. dissertation was the design of microelectromechanical silicon filters and resonators for radiocommunications. Since 2005 he is an Associate Professor in University Paris-VI (Pierre et Marie Curie), France, in the LIP6 laboratory. His research interests include study, modeling and design of nonlinear integrated circuits for sensor interface and for mixed-signal applications.

Philippe Basset received the engineering diploma in electronics from ISEN Lille, France, in 1997 and the M.Sc. and Ph.D. degrees from IEMN University of Lille in 1999 and 2003, respectively. In 2004 he was a Postdoc at Carnegie Mellon University, Pittsburgh, PA, USA. In 2005 he joined ESIEE Paris at the Université Paris-Est, France, where he is currently an Associate Professor. His research interests include micro/nanostructuration of silicon and micropower sources for autonomous MEMS. He led several projects on energy harvesting using micro- and nanotechnologies and he serves in the TPC of the PowerMEMS conference since 2013. Member of the ESYCOM laboratory, he is currently leading the Sensors and Measuring MEMS group.