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Full paper

MEMS four-terminal variable capacitor for low power capacitive adiabatic logic with high logic state differentiation

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ABSTRACT

This paper presents a novel four-terminal variable capacitor (FTVC) dedicated to the recent concept of low power capacitive adiabatic logic (CAL). This FTVC is based on silicon nano/micro technologies and is intended to achieve adiabatic logic functions with a better efficiency that by using field effect transistor (FET). The proposed FTVC consists of two capacitors mechanically coupled and electrically isolated, where a comb-drive input capacitor controls a gap-closing capacitor at the output. To fully implement the adiabatic combinational logic, we propose two types of variable capacitors: a positive variable capacitor (PVC) where the output capacitance value increases with the input voltage, and a negative variable capacitance (NVC) where the output capacitance value decreases when the input voltage increases. A compact and accurate electromechanical model has been developed. The electromechanical simulations demonstrate the ability of the proposed FTVC devices for CAL, with improved features such as high logic states differentiation larger than 50% of the full-scale input signal and cascability of both buffers and inverters. Based on the presented analysis, 89% of the total injected energy in the device can be recovered, the remaining energy being dissipated through mechanical damping. During one cycle of operation, a buffer gate of $10 \times 2.5\,\mu m^2$ dissipates only 0.9fJ.

1. Introduction

A digital electronic circuit can be considered as a chain of interconnected elementary blocks [1], each of them having an input capacitance C_o corresponding to the gate capacitor of a field effect transistor (FET) and some parasitic interconnections. In current CMOS technology, the classical combinational logic is based on the abrupt charge and discharge of C_o through PMOS and NMOS transistors for coding a logic state, as in the CMOS inverter (Fig. 1a). When changing from “0” to “1” logic state ($V_{in} \rightarrow 0$), C_o is charged from the power supply V_{CC} through the PMOS resistance in on-state R_{on}, while the NMOS is in its cut-off region (Fig. 1b). During this operation, the energy provided by the source is given by $QV_{CC} = C_oV_{CC}^2$: half of it is dissipated through R_{on} and the other half is stored in C_o. When changing from “1” to “0” ($V_{in} \rightarrow 1$), C_o is now discharged to the ground through the NMOS transistor in ON state (Fig. 1c). The energy previously stored in C_o is now dissipated into the ground and the total energy provided by the source is eventually fully dissipated.

In addition to the active power dissipation $C_oV_{CC}^2f$, where f is the operating frequency, there are dissipation due to the short-circuit transition and the sub-threshold leakage $I_{leak}V_{CC}$, where I_{leak} is the sub-threshold leakage current. The short-circuit transition power corresponds to about 10% of the average power and is typically the smallest contribution to the losses [3–5]. Though among all VLSI logic families, CMOS circuits have the lowest power dissipation [2,3], reducing the energy consumption is one of the main concerns in modern integrated circuits (IC). It can be reduced by (i) developing devices with higher sub-threshold slope, (ii) reducing C_o and (iii) working at low frequency. Reducing C_o is limited by the lithography. Reducing the supply voltage V_{CC} is a powerful method but this solution has limits related to the transistor size reduction [6]. Consequently, the dissipation cannot be reduced significantly.

In the early sixties, Landauer stated that to erase one bit of known information, which is consider as the most basic computing event, it requires the dissipation of at least k_B. T.ln(2), where k_B is the Boltzman constant and T is the temperature in Kelvin [7]. At room temperature, it corresponds to 18 meV. However, to overcome the energy barrier due to the thermal noise, a minimum of 100.k_B. T (~ 2.6 eV at 300°K) is required [8]. As a comparison, the current dissipated energy at each switching event, with the 10 nm CMOS technology, is given by $0.5C_oV_{cc}^2$ ~ 40 eV, which is about 3 orders of magnitude above the Landauer limit and one order of magnitude above the thermal noise

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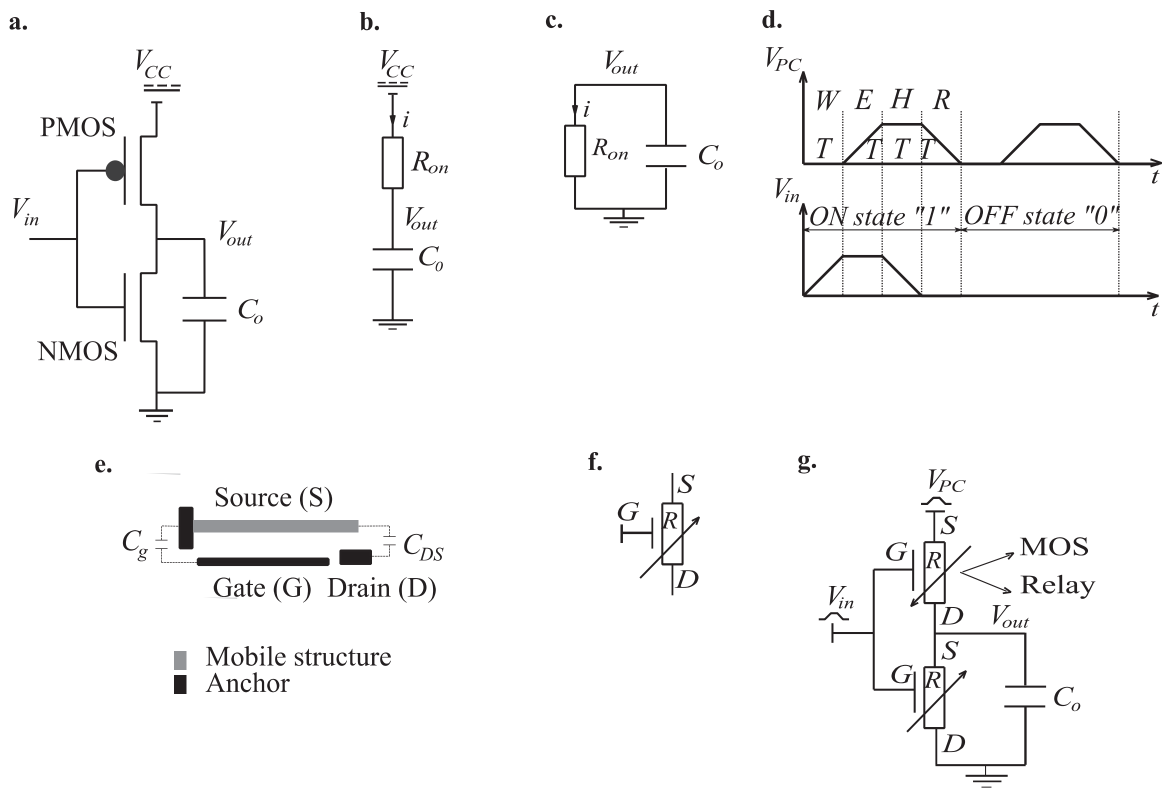

Fig. 1. From classical CMOS inverter to inverter based on adiabatic logic. a) Schematic of a conventional CMOS inverter. b) Equivalent circuit in charging phase. c) Equivalent circuit in discharging phase. d) PC circuit signals. e) Implementation of a resistive electromechanical relay and f) its schematic representation. g) Schematics of an adiabatic resistive inverter.

limit.

A good way to even further reduce the power consumption is the adiabatic logic approach [6,9], which can be combined with the concept of "energy recovery" [10]. It consists in charging the gate capacitor with a constant current, instead of a constant voltage as in classical digital circuits, then to recover the injected charge when going back to the initial state. It results in an optimized power dissipation [11] but requires a dynamic logic: the charge and discharge of C_o have to be performed by a ramped supply voltage signal V_{PC} called the Power Clock (PC).

1.1. Dissipated energy in CMOS adiabatic logic

The principle of the adiabatic logic is detailed in [6,9]. To explain the principle of operation of an adiabatic logic gate, let us consider the schematic of the inverter gate in Fig. 1a. The PC signal is typically divided into 4 equal steps of equal duration T, that we named the *Evaluate* (E), *Hold* (H), *Recovery* (R) and *Wait* (W) intervals. Consequently, a logic "1" state at the input voltage V_{in} is not a DC voltage value anymore as well. It corresponds to the power clock signal but shifted by a quarter of period T, as shown in Fig. 1d.

During the charging phase (*Evaluate* stage), the supply voltage is ramped from 0 to V_{CC} within the charging time T, and the current i is determined by:

$$i = C_o \frac{dV_{PC}}{dt} = C_o \frac{V_{CC}}{T} \tag{1}$$

The energy dissipated through R_{on} during the charging and discharging phases is then given by:

$$E_{dynamic} = 2i^2 R_{on} T = 2\left(\frac{C_o V_{CC}}{T}\right)^2 R_{on} T = 2\frac{R_{on} C_o}{T} C_o V_{CC}^2 \tag{2}$$

If the time constant $2R_{on}C_o$ is lower than T, the energy dissipation is reduced compared to the energy dissipation $C_o V_{CC}^2$ in classical CMOS circuits. The ramp duration of the PC (also equal to T) strongly affects the Joule dissipation: $E_{dynamic}$ vanishes for long charging times. Similarly, scaling down the supply voltage and reducing the capacitance load also reduce the dissipated energy in adiabatic logic, as we mentioned earlier.

In addition, it exits a non-adiabatic energy associated to the incompressible threshold voltage V_{th} of the MOS transistor equal to:

$$E_{non-adiabatic} = \frac{1}{2} C_o V_{th}^2, \tag{3}$$

And a leakage current can flow from the supply voltage to the ground through the disable transistors due to the semiconductor technology, leading to a static energy dissipation given by:

$$E_{static} = \frac{((\bar{I}_{leak}))V_{CC}}{f} \tag{4}$$

where $\bar{I}_{leak}$ is the mean leakage current.

By taking into account the (adiabatic) dynamic losses, the (static) leakage and the (uncompressible) non-adiabatic losses, we can express the total energy dissipation of an adiabatic inverter gate based on CMOS transistors as:

$$E_{Total} = 2\frac{R_{on} C_o}{T} C_o V_{CC}^2 + \frac{1}{2} C_o V_{th}^2 + \bar{I}_{leak} V_{CC} \frac{1}{f} \tag{5}$$

1.2. Electromechanical devices to reduce the non-adiabatic losses

Nano-Electromechanical relays (NEMS relays) have been proposed to replace CMOS transistors in order to reduce the static and non-adiabatic losses. Most of them are electrostatically actuated [12,13] but a nanomagnetic switch could also be used [8]. These nanorelays need low switching energy and promise perfect isolation with zero leakage current in the OFF state. They have already been evaluated for classical logic [14,15] and even tested with an integrated circuit [16]. In addition, they can be used efficiently for the adiabatic logic [17].

A classical NEMS relay has typically three terminals, the gate (G), the source (S) and the drain (D) (Fig. 1e). It consists in an electrostatic actuator made of a flexible beam S and a fixed electrode G, forming a variable capacitance C_g (Fig. 1e). The voltage across C_g determines the state of the relay. In the OFF state, C_g is low and the resistance R between the drain and the source is infinite (open circuit). When an input voltage is applied between S and G, the beam deflects and creates a resistive contact between the drain and the source (ON states). Consequently, the relay can be seen as a capacitor controlling a variable resistor, represented with the symbol in Fig. 1f. To implement all combinational logic, we need two types of relay: normally-ON and normally-OFF relays to replace the NMOS and PMOS transistors in integrated circuits respectively. Fig. 1g illustrates how the relays (or the MOS transistors) can be implemented in an adiabatic inverter.

However, the unavoidable contact resistance of resistive micro/nano-electromechanical relays, their poor mechanical reliability and their low switching frequencies have been highlighted in literature [12–17]. In order to avoid the resistive contact in the on-state and to reduce the dynamic dissipation, a purely capacitive electromechanical switch could be a better solution [18]. Based on this new paradigm, the so-called *Capacitive Adiabatic Logic* (CAL), Galisultanov et al. have detailed in [19] the concept of a fully contact-less electromechanical device for the CAL. In this paper we described new four-terminal variable capacitors (FTVC) for the CAL that still have a contact zone but present several major advantages, like a better differentiation between a "0" and a "1" logic state, a higher frequency of operation or a smaller area. In addition, based on our simulations, we demonstrated for the first time the ability to cascade several devices.

The organization of the paper is as follows. In the next section, we detail these new FTVC and their mathematical models that can be used to implement the CAL approach. In Section 3, we analyze the different energy losses of the proposed configurations. We conclude with the demonstration of the operation of cascaded elementary combinational gates.

2. Proposed architectures for the CAL devices

2.1. General description

In the *Capacitive Adiabatic Logic* approach, the resistive elements (transistors or relays) are replaced by purely capacitive elements. Similarly to the resistive-based adiabatic logic, the logic function required an input capacitance C_g between the gate G and the ground, and an output capacitance C_{DS} between the terminals D and S (we use the FET transistor notation, i.e. the input voltage V_{in} is applied between the gate and the ground). The only difference is that the electrodes of C_{DS} are never in ohmic contact. All the terminals are electrically isolated, but two of them (G and S) are mechanically connected. Two types of output variable capacitances are needed to fully implement the adiabatic combinational logic: *Positive Variable Capacitances* (PVC) where C_{DS} increases with the control voltage V_{in} and *Negative Variable Capacitances* (NVC) where C_{DS} decreases when V_{in} increases.

In the following, we propose implementations for a PVC and a NVC that can be fabricated in silicon micro/nanotechnologies. Each device consists of an electrostatic comb-drive actuator for the input capacitance C_g and a gap-closing (possibly with interdigited-combs) for the output capacitor C_{DS}. The capacitance C_g and C_{DS} are mechanically connected but electrically separated by a dielectric. Fig. 2a shows a schematic top-view of a practical buffer using a PVC and Fig. 2b depicts an inverter with a NVC, both in the OFF state. Fig. 2c,d,e give more geometric details of C_g, the spring mechanical suspensions and C_{DS} respectively.

2.2. Principle of the PVC configuration

Let's assume that the buffer in Fig. 2a is loaded with the signals presented in Fig. 1d. In the OFF state ($V_{in}=0$), the electrodes S and D are separated by d_{max}, and the capacitance C_{DS} is minimum (Fig. 3a). When V_{in} is applied (ON state), the comb-drive moves the rotor in the $\vec{x}$ direction, resulting in an increase of C_g and C_{DS}. According to the capacitor divider {C_o-C_{DS}}, the output V_{out} follows V_{PC}. The electrical force F_e, created by the voltage $V_{DS}=V_{PC}$-V_{out}, is opposed to the mechanical spring force F_m (Fig. 3b). Consequently, during the *Hold* interval when V_{in} decreases, F_e balances F_m and the equilibrium is maintained: C_g and C_{DS} remain constant, allowing V_{out} to still follow V_{PC}.

2.3. Principle of the NVC configuration

Now we consider the inverter in Fig. 2b loaded with the same signals in Fig. 1d. In the OFF state ($V_{in}=0$), C_{DS} is maximal because S and D are separated by d_{min}, the thickness of a dielectric layer covering the electrodes (Fig. 3c). When V_{in} is applied (ON state), the comb-drive moves the rotor in the $\vec{x}$ direction, resulting in an increase of C_g and a decrease of C_{DS}. This time, the electrical force F_e and spring force F_m are in the same direction (Fig. 3d). Consequenctly, during the *Hold* interval when V_{in} decreases, the mobile electrode may return to its initial position causing an incorrect operation. To avoid this problem, we proposed to add an additional electrode M connected to the ground and forming with S a capacitance C_{SM}. The voltage across C_{SM} creates an additional electrical force F_e' that balances the other forces and the equilibrium can be maintained (Fig. 3e,f).

2.4. The adiabatic conditions

2.4.1. Conditions related to input signals

In order to satisfy the adiabatic conditions, the inputs have to be stable during ramp-up and ramp-down phases of the PC, and the durations of the *Evaluate*, *Hold*, and *Wait* phases of both input and power-clock signals have to be equal [20,21]. Therefore, as already stated in the introduction, a four-phase power clock consisting in four equal intervals T is required, and the input signal is shifted by a quarter of period with respect to the PC. In the ON state, the following rules have to be followed :

(i) During the *Wait* interval, V_{in} ramps up, C_g increases and reaches its maximum value at the end of the interval. As soon as C_g increases, C_{DS} evolves depending on the gate configuration: for a PVC, it increases until its maximum and for the NVC, it decreases to its lower value.

(ii) During the *Evaluate* interval, V_{PC} increases and V_{in} remains constant at its high value. In the PVC configuration, the output V_{out} follows the PC and the capacitance node C_o starts to charge. In the NVC, the output remains at a low level.

(iii) During the *Hold* interval, V_{in} decreases but V_{PC} remains high, and then the variables capacitances C_g and C_{DS} doesn't change (thanks to the help of electrode M for the NVC).

(iv) During the *Recover* interval, V_{PC} decreases while V_{in} remains grounded. The mechanical equilibrium is holded until low value of V_{PC}, thanks to the typical hysteresis in electrostatic transducers [23]. Both C_g and C_{DS} remain constant till then, and the charge stored in C_o can be recovered by the source.

To build a circuit, the CALs gates are cascaded and each gate is supplied by a PC, as shown in Fig. S1. Since the output signal follows the PC, two subsequent PC should be delayed by a quarter of period to satisfy the adiabatic conditions. Therefore, a four-phase power-clock (V_{PC1} to V_{PC4}) is needed to cascade several gates.

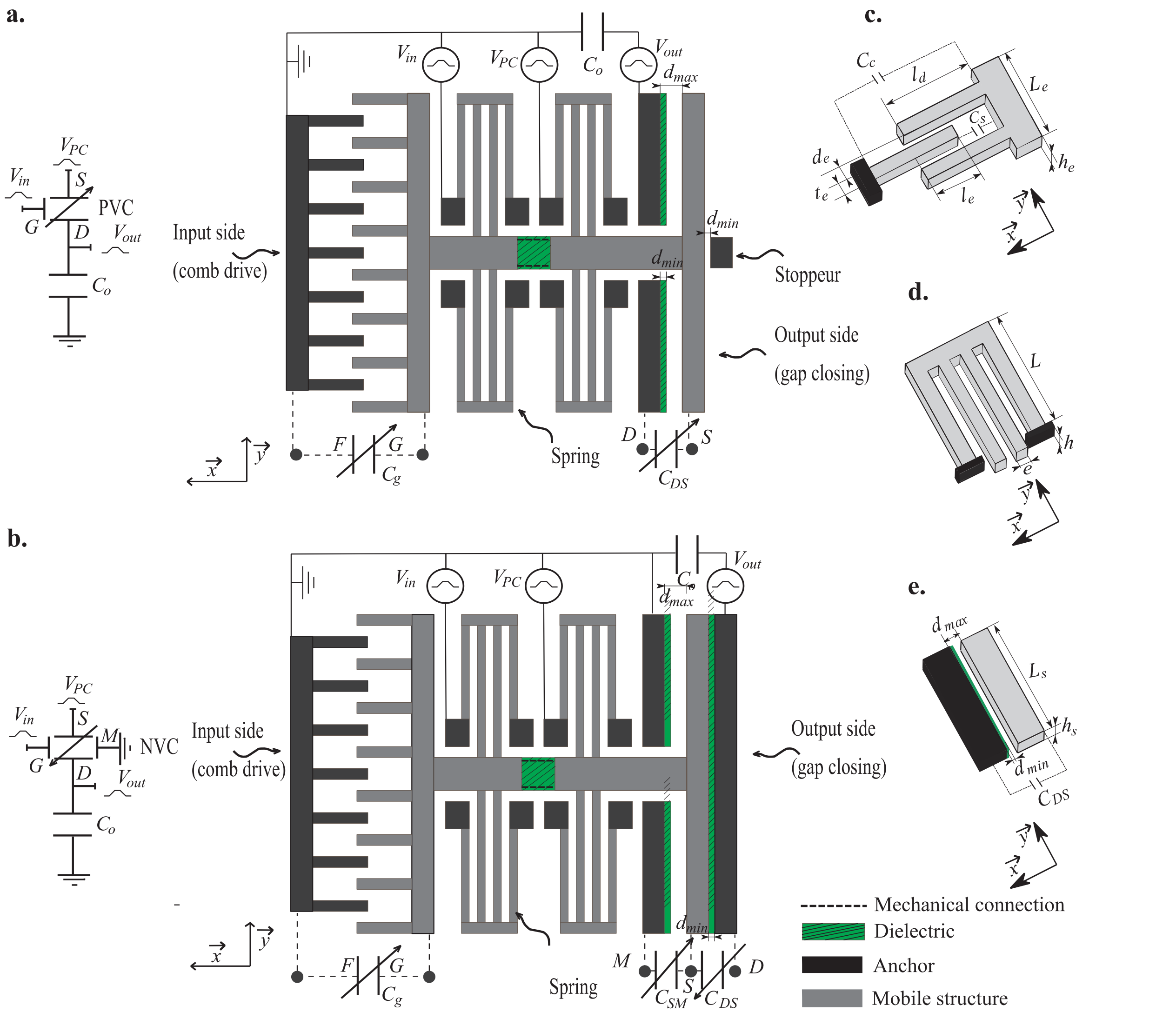

Fig. 2. Electromechanical implementations of FTVC in the OFF state. a) Electromechanical implementation of a buffer with a PVC. b) Implementation of an inverter with a NVC. c) Geometric details for the comb-drive capacitance C_g for $n_e = 1$. d) Geometric details for a spring. e) Geometric details for the gap-closing capacitance C_{DS}.

2.4.2. Conditions related to C_{DS}

Fig. 4 shows schematic representations of a buffer and an inverter. The PVC design has four terminals while NVC has five, since it includes the additional electrode M. The electrical equations are given by:

$$V_{PC} = V_{DS} + V_{out} \tag{6}$$

$$i = C_{DS}\frac{dV_{DS}}{dt} + V_{DS}\frac{dC_{DS}}{dt} = C_o\frac{dV_{out}}{dt} \tag{7}$$

where V_{DS}, C_o, and i are the voltage across the drain and source of either PVC or NVC, the input capacitance of the following gate and the current provided by the power clock respectively. We can deduce the instantaneous logic output voltage as:

$$V_{out} = V_{PC}\frac{C_{DS}}{C_{DS} + C_o} \tag{8}$$

Since the input voltage V_{in} controls the value of C_{DS}, it also controls the voltage ratio between the power-clock signal and the output node through the capacitor bridge divider $\{C_{DS}\text{-}C_o\}$. The values of C_{DS} have to be carefully chosen: the minimum value of C_{DS} has to be small compared to C_o in order to obtain the low logic state, and the maximum value of C_{DS} has to be high compared to C_o to achieve the high logic level.

2.5. Modeling the CAL devices

2.5.1. Modeling the input capacitance variation

Various models can be found in the literature to model capacitances and their fringe fields. In this work, we use the Mejis-Fokkema formula [22] for the comb-drive C_g and the Palmer formula [24] for the gap-closing capacitances C_{DS} and C_{SM}.

For C_g (Eq. (9)), the first term C_c represents the lateral capacitance without fringing effect, C_f estimates the fringe capacitance and C_s is the capacitance at the tip of fingers (c.f. Fig. 2c):

$$C_g = 2C_c + C_f + C_s \tag{9}$$

$$C_g = \frac{2n_e\varepsilon h_e(l_e+x)}{d_e} + 2n_e\varepsilon h_e\left[0.77 + 1.06\left(\frac{l_e+x}{d_e}\right)^{1/4} + 1.06\left(\frac{h_e}{d_e}\right)^{1/2}\right] + \frac{2n_e\varepsilon h_e t_e}{l_d - l_e - x} \tag{10}$$

where n_e and h_e represents the comb's finger numbers and their thickness respectively. l_e, d_e, l_d and t_e are the initial overlapping distance between the fingers, the initial gap distance between the fixed and movable fingers, the length and width of the finger respectively. ε is the air permittivity and x is the displacement in the $\vec{x}$ direction. This

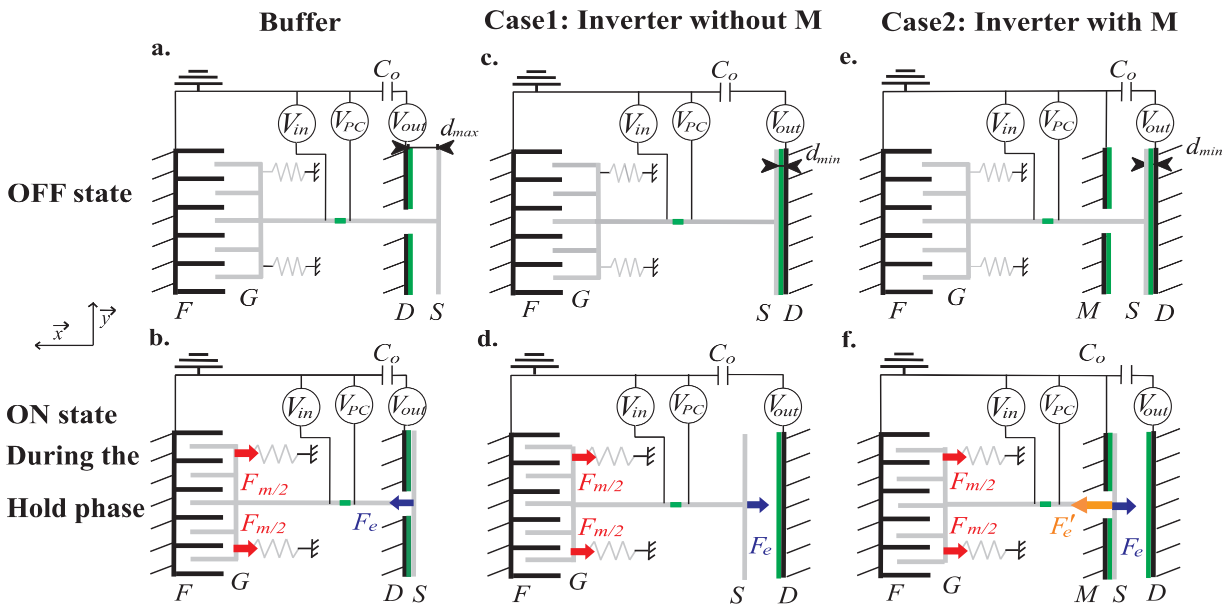

Fig. 3. Different states of the buffer (PVC) and the inverter (NVC). a) Buffer in the OFF state. b). Buffer in the ON state during the Hold phase. c) Inverter without M in OFF state. d) Inverter without M in the ON state during the Hold phase. e) Inverter with M in OFF state. f) Inverter with M in the ON state during the Hold phase.

model is in good agreement with the commercial software MEMS+ from Coventor ware (cf Fig. S2)

2.5.2. Modeling the ouput capacitance variation

The gap-closing capacitance C_{DS} is given by the Palmer formula [24], (Eq. (11)) and (Eq. (12)) for PVC and NVC respectively:

$$C_{DSPVC} = \frac{n_s h_s L_s \varepsilon}{d_{max} - x}\left[1 + 2\left(\frac{d_{max} - x}{h_s \pi}\right)\left(1+\log\left[\frac{h_s \pi}{d_{max} - x}\right]\right)\right] \tag{11}$$

$$C_{DSNVC} = \frac{n_s h_s L_s \varepsilon}{d_{min} + x}\left[1 + 2\left(\frac{d_{min} + x}{h_s \pi}\right)\left(1+\log\left[\frac{h_s \pi}{d_{min} + x}\right]\right)\right] \tag{12}$$

The expression of C_{SM} is similar to the expression of C_{DS} in PVC, and is expressed by:

$$C_{SM} = C_{DSPVC} = \frac{n_s h_s L_s \varepsilon}{d_{max} - x}\left[1 + 2\left(\frac{d_{max} - x}{h_s \pi}\right)\left(1+\log\left[\frac{h_s \pi}{d_{max} - x}\right]\right)\right] \tag{13}$$

where n_s, h_s, L_s , d_{max} or d_{min} are the number of C_{DS} electrodes, their thickness, their length and their initial gap distance respectively.

2.5.3. Modeling the device dynamics

From the Newton's second law, the dynamic behavior of the PVC and NVC structures is represented by the non-dimensional equation (Eq. (14)). The first term is associated to the kinetic force, the second term is associated to the mechanical damping force, the third one is related to the spring force, the fourth one represents the electrical force from C_g and the next one is the electrical force from C_{DS}. The last term represents the electrical force associated to C_{SM} for the NVC structure. The non-dimensional variables used in (Eq. (14)) are given in Table 1.

$$\ddot{\hat{x}} + \lambda\dot{\hat{x}} + \hat{x} - (\hat{V}_{in})^2\left(1+\frac{1}{(\beta_1 - \hat{x})^2} + \frac{\gamma}{(\beta_2 + \hat{x})^{0.75}}\right) + \alpha\left[\alpha_1 \hat{V}_{DS}^{\,2}\left(\frac{1+\beta_4(\beta_5 + \hat{x})}{(\beta_5 + \hat{x})^2}\right) - \alpha_2(\hat{V}_{PC})^2\left(\frac{1+\beta_4(\beta_3 - \hat{x})}{(\beta_3 - \hat{x})^2}\right)\right] = 0 \tag{14}$$

where $\gamma = 0.265$, $\beta_4 = \frac{2d_e}{h_s}$, $\alpha = \frac{n_s h_s L_s}{2 n_e h_e d_e}$, $\alpha_1 = -1$ and $\alpha_2 = 0$, for PVC configuration and $\alpha_1 = \alpha_2 = 1$ for NVC.

2.5.4. Modeling the impact

At each impact between the drain and the source electrodes, the

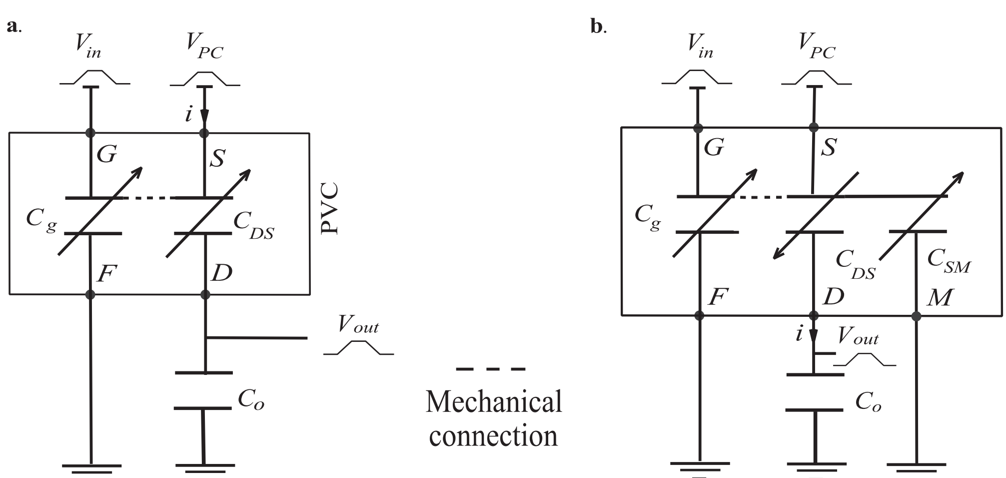

Fig. 4. Equivalent circuit of a) a CAL buffer, and b) a CAL inverter.

Table 1
Non-dimensional variables.

Variable	Description
$\hat{x} = x/d_e$	Displacement in the direction $\vec{x}$
$\hat{t} = t\sqrt{k_x/m}$	Time
$\lambda = c/\sqrt{m.\ k_x}$	Damping
$\beta_1 = (l_d - l_e)/d_e$	Gap of the side capacitance C_s
$\beta_2 = l_e/d_e$	Overlapping distance between fingers
$\beta_3 = d_{max}/d_e$	Initial gap of PVC C_{DS}
$\beta_5 = d_{min}/d_e$	Initial gap of NVC C_{DS}.
$\hat{V}_{in} = \mu V_{in}$	Input signal, where $\mu = \sqrt{\frac{\varepsilon n_e h_e}{k_x d_e^2}}$
$\hat{V}_{PC} = \mu V_{PC}$	Power Clock signal
$\hat{V}_{DS} = \mu V_{DS}$	Signal across the output capacitance C_{DS}
$\hat{V}_{CC} = \mu V_{CC}$	Maximal supply voltage of different signal
$\hat{E}_m = E_m/\alpha_1$	Mechanical energy where $\alpha_1 = k_x d_e^2$
$\hat{E}_{in} = E_{in}\mu^2 \quad /C_o$	Input energy produced by the input source where
$\hat{E}_{Cg} = E_{Cg}\mu^2 \quad /C_o$	Electrical energy stored in the input capacitance C_g
$\hat{E}_{PC} = E_{PC}\mu^2 \quad /C_o$	Electrical input energy produced by the Power clock
$\hat{E}_{CT} = E_{CT}\mu^2 \quad /C_o$	Electrical energy stored in C_{DS} and C_o
$\hat{C}_g = C_g/C_o$	Input capacitance
$\hat{C}_{DS} = C_{DS}/C_o$	Output capacitance

Table 2
Physical and geometric parameters used in simulations.

Variable	Description	Value
E	Yong's modulus of silicon (N/m^2)	$169\ 10^9$
ε	Permittivity of air (F/m^3)	$8.854\ 10^{-12}$
L_s	Length of the gap closing capacitance C_{DS} (µm)	8.72
h_s	Thickness of the gap closing capacitance C_{DS} (µm)	0.4
h_e	Thickness of the comb-drive capacitance C_g (µm)	0.4
d_{max}	Initial gap distance of C_{DS} (µm)	0.25
d_{min}	Thickness of the dielectric (µm)	0.01
n_s	Number of the gap-closing capacitance C_{DS}	1
n_e	Number of finger in C_g	55
L	Length of the mechanical suspension (µm)	5
e	Width of mechanical suspension (µm)	0.02
h	Thickness of mechanical suspension (µm)	0.4
L_e	Length of the comb-drive capacitance C_g (µm)	8.8
d_e	Gap distance of the comb-drive capacitance C_g(µm)	0.04
t_e	Width of the finger of the comb-drive capacitance C_g (µm)	0.04
l_e	Overlapping distance between fingers of C_g (µm)	0.02
l_d	Length of the finger of the comb-drive capacitance C_g (µm)	0.4
m	Effective mass of the movable part (Kg)	$1.98\ 10^{-14}$
K_x	Spring constant in the direction $\vec{x}$ (N/m)	0.02
c	Damping (Kg/s)	$1.96\ 10^{-8}$
C_o	Load capacitance (fF)	1

mobile electrode losses a small part of its kinetic energy during a bouncing phenomenon. During successive contacts, the velocity can be expressed as [25,26]:

$$\dot{\hat{x}}_n = -K_{loss}\dot{\hat{x}}_{n-1} \tag{15}$$

where $\dot{\hat{x}}_{n-1}$ and $\dot{\hat{x}}_n$ are the velocities before and after the n^{th} impact, and K_{loss} is the coefficient of restitution. When the mobile electrode reaches the contact, its velocity is set according to (Eq. (15)). The characteristics of the bounces depend on the mass of the mobile part and its velocity, the elastic response of the material and the surface hardness [26].

3. Simulations and analysis

In this section, we present and analyze the simulations of Capacitive Adiabatic Logic circuits using the MEMS devices presented previously. The physical and geometrical features of the proposed implementations are given in Table 2. These dimensions are carefully chosen in order to match the FET transistor parameters. First, we present how a buffer or an inverter works. Then we study the energy transfer and losses in a buffer gate. Finally, we demonstrate the possibility to cascade in series several buffers or inverters.

In the following, a “1” adiabatic logic input (i.e. the “ON state”) corresponds to a 4-interval pulse similar to V_{PC}, but with a phase shift of a quarter of period in order to satisfy the adiabatic logic conditions. A “0” (“OFF state”) means $V_{in} = 0$ during the entire sequence (Fig. 1d).

4. Analysis of a single gate

4.1. Simulation of a buffer

In order to understand how a CAL buffer works, we plotted in Fig. 5b the output voltage of a PVC and the displacement of its mobile part for the input logic sequence “1 0” shown in Fig. 5a. C_o is set to 1 fF according to [1]. During the “1” state, as soon as V_{in} increases (*Wait* interval), the comb-drive at the input moves the mobile part, $d_s = d_{max}$-x decreases and C_{DS} increases from its minimum to its maximum value, with a short oscillation induced by the impact of the mobile mass onto the rigid frame. Then, during the *Evaluate* interval, $V_{in,}$ and so C_{DS} are constant, while V_{PC} increases. C_{DS} is at its maximum value and V_{out} follows V_{PC} through the constant capacitive divider formed by the {C_{DS}-C_o} couple. This lasts even beyond the *Hold* interval, while V_{in} decreases till 0V, because of the electrostatic force F_e across C_{DS} introduced by V_{PC} is still higher than the restoring force of the mechanical springs F_m. This memory effect corresponding to the hysteresis of electrostatic transducers [23] is important to keep C_{DS} at its maximum value, allowing V_{out} to follow the PC. During the *Recovery* interval, V_{out} progressively decreases with V_{PC}, and at some point the electrostatic force associated to C_{DS} is not sufficient to compensate the restoring spring force, so C_{DS} rapidly decreases to its minimum value, bringing V_{out} definitely to 0 V.

Then the “0” state starts. V_{in} remains equal to 0 during the 4 intervals of V_{PC} and the electrostatic force across C_g is null. However, when V_{PC} increases during the *Evaluate* interval, its associated electrostatic force leads to a small variation of C_{DS} that is not negligible compare to C_o, so we can observe a small variation of V_{out} following the evolution of V_{PC}. In addition, we can also observe a tiny increase of C_{DS} due to the electrostatic force across C_{DS} introduced by V_{PC}. However V_{out} has to remain below the threshold voltage corresponding to the “0” logic state.

4.1.1. Simulation of an inverter

Similarly, the time history of a NVC loaded with a capacitor C_o of 1 fF is given in Fig. 5c and d for the same “ 1 0” logic input. At $t = 0$, C_{DS} is at its maximum and V_{in} starts to increase from 0 V to V_{CC} (*Wait* interval). V_{out} is initially equal to 0 V, so the mobile electrode easily moves with the increase of V_{in}, and C_{DS} quickly decreases to its minimum value. During the *Evaluate* interval, V_{in} and so C_{DS} remain constant. Since V_{PC} increases and C_{DS} is not negligible, V_{out} follows V_{PC} but has to remain below the maximum voltage allowed for a “0” logic level. During the following *Hold* interval, V_{in} decreases. First C_{DS} remains at its minimum because the electrostatic force across C_g is still higher that the spring restoring force. However, at some point, this is not the case anymore. Then C_{DS} increases, while V_{PC} is still high, which leads to an unexpected increase of V_{out} before the next “0” logic at the input (case 1 Fig. 5c). To avoid this, we added the M electrode connected to the ground that creates an additional electrostatic force across C_{SM}, controlled by V_{PC} and opposed to the spring force (Fig. 3e,f). Hence, C_{DS} can be maintained at its minimum value during the whole *Hold* interval (case 2 Fig. 5d).

Close to the end of the *Recover* interval, while V_{PC} is small enough, the mobile part progressively moves back to its initial position. Simultaneously C_{DS} progressively gets back to its maximum value, which is reached at the beginning of the *Wait* interval. Hence V_{out} is

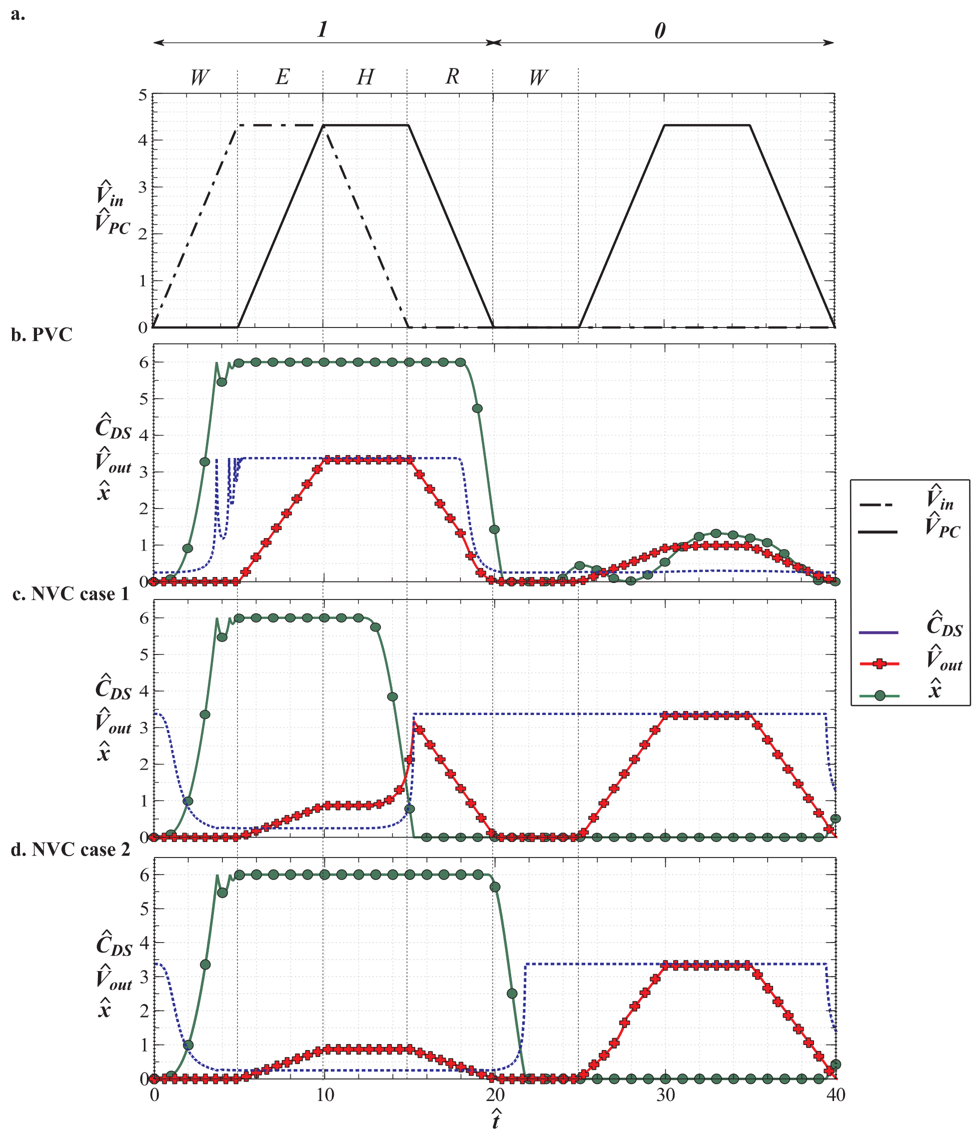

Fig. 5. Operation of simple gates for a "1 0" logic input. a) the input and PC signals. b) Simulation of a CAL buffer. c) Simulation of a CAL inverter without electrode *M* (case 1) and d) with electrode *M* (case 2). All dimensions are given in Table 1.

always bellow the "1" logic state before the end of the "1" sequence at the input.

4.2. Energy analysis

In this section, we investigate the energy balance of the design and we show that only a small part of the energy provided by the electrical sources cannot be recovered.

C_g and C_{DS} are two electromechanically coupled transducers having two electrical inputs and one mechanical output (Fig. 6a). The instantaneous electrical energy is given by:

$$E_e(t) = E_{in} + E_{PC} = \int (V_{in} i_{in} + V_{PC} i_{PC}) dt \tag{16}$$

$$= \int [V_{in} i_{in} + (V_{DS} + V_{out}) i_{PC}] dt$$

The instantaneous mechanical energy output of the system is given by:

$$E_m(t) = \int f(t) \dot{x}(t) dt \tag{17}$$

where $f(t)$ is the mechanical force applied on the mobile part and $\dot{x}(t)$ is its velocity. The expression of i_{in} and i_{PC} are given by:

$$i_{in} = \frac{d(C_g V_{in})}{dt} = C_g \frac{dV_{in}}{dt} + \frac{dC_g}{dx} V_{in} \frac{dx}{dt} = C_g \frac{dV_{in}}{dt} + \frac{dC_g}{dx} V_{in} \dot{x}(t), \tag{18}$$

$$\begin{aligned} i_{PC} &= \frac{d(C_{DS} V_{DS})}{dt} = C_{DS} \frac{dV_{DS}}{dt} + \frac{dC_{DS}}{dx} V_{DS} \frac{dx}{dt} \\ &= C_{DS} \frac{dV_{DS}}{dt} + \frac{dC_{DS}}{dx} V_{DS} \dot{x}(t) = C_o \frac{dV_{out}}{dt} \end{aligned} \tag{19}$$

Combining equations (Eq. 10), (Eq. (12)) and (Eq. (13)), the expression of $E_e(t)$ becomes:

$$E_e(t) = \frac{C_g}{2} {V_{in}}^2 + \frac{C_{DS}}{2} {V_{DS}}^2 + \frac{C_o}{2} {V_{out}}^2 + \int \left(\frac{dC_g}{dx} {V_{in}}^2 + \frac{dC_{DS}}{dx} {V_{DS}}^2 \right) \dot{x}(t) dt \tag{20}$$

$$= \frac{C_g}{2} {V_{in}}^2 + \frac{C_o}{2} {V_{out}}^2 + \frac{C_{DS}}{2} {V_{DS}}^2 + E_m = E_{Cg} + E_{Co} + E_{CDS} + E_m$$

The first three terms of (Eq. (20)) represent the electrostatic energy stored in the capacitances C_g, C_o and C_{DS} respectively. The last term E_m represents the mechanical energy. In other words, the electrical energy supplying a capacitive transducer is converted in two parts, the electrostatic energy stored in the variable capacitance and the output mechanical energy [27,28].

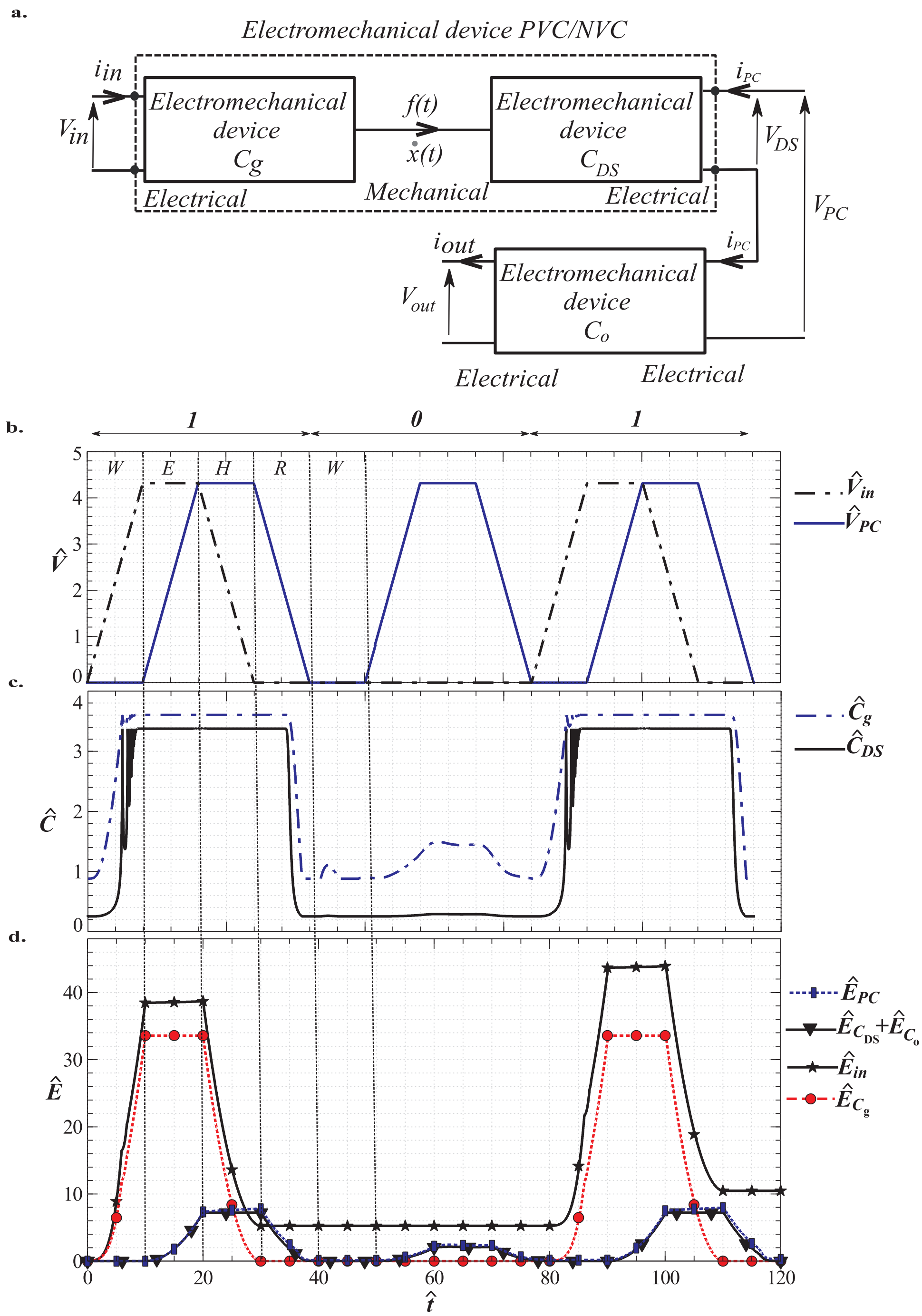

Fig. 6. Energy Analysis of a buffer. a) Block-schematic representation of a gate (PVC or NVC). b) Evolution a the buffer's input voltages. c) Evolution of capacitances $\hat{C}_g$ and $\hat{C}_{DS}$. d) Energy contributions of electrical parts.

We have investigated the energy conversion and losses in the CAL buffer shown in Fig. 4a, and loaded by a logical sequence V_{in} (101) (Fig. 6b). The variations of $\hat{C}_{DS}$ and $\hat{C}_g$, the non-dimensional values of C_{DS} and C_g (see Table 1) are shown in Fig. 6c. During the *Wait* interval, V_{in} increases and a large part of the electrical input energy E_{in} is stored in C_g (we call it E_{Cg}). The rest is converted into the mechanical energy E_m: part of it is stored in the mechanical springs that moves the body, leading to an increase of C_g and C_{DS} until they reach their maximum values. The remaining energy is converted into kinetic energy and part of it is lost during the impact between the drain and the source electrodes (see the oscillations of $\hat{C}_{DS}$ and $\hat{C}_g$ in Fig. 6c). During the *Evaluate* interval, V_{PC} increases, generating an electrical input energy E_{PC}. However C_g and C_{DS} remain maximum and there is no electromechanical energy conversion: all the electrical energy E_{PC} is stored in C_{DS} and C_o.

During the *Hold* interval, V_{in} decreases but the capacitances C_{DS} and C_g do not change, as explained previously: only E_{Cg} is recovered by V_{in}. During the *Recovery* interval, both electrical energies stored in C_{DS} and C_o are recovered by V_{PC}, and C_{DS} remains constant for a while.

The electrical energy necessary to supply the buffer is not fully recovered: some energy is dissipated by damping losses and during the impact. Fig. 6d shows the evaluation of the non-dimensional electric energy $\hat{E}_{in}$ produced by the source V_{in} , the energy $\hat{E}_{Cg}$ stored in C_g, the energy $\hat{E}_{PC}$ produced by the source V_{PC} and the energy ($\hat{E}_{C_{DS}}$ + $\hat{E}_{C_o}$) stored in both capacitances C_{DS} and C_o. During one cycle, with the dimension in Table 2 corresponding to a realistic device of 25 μm^2, the

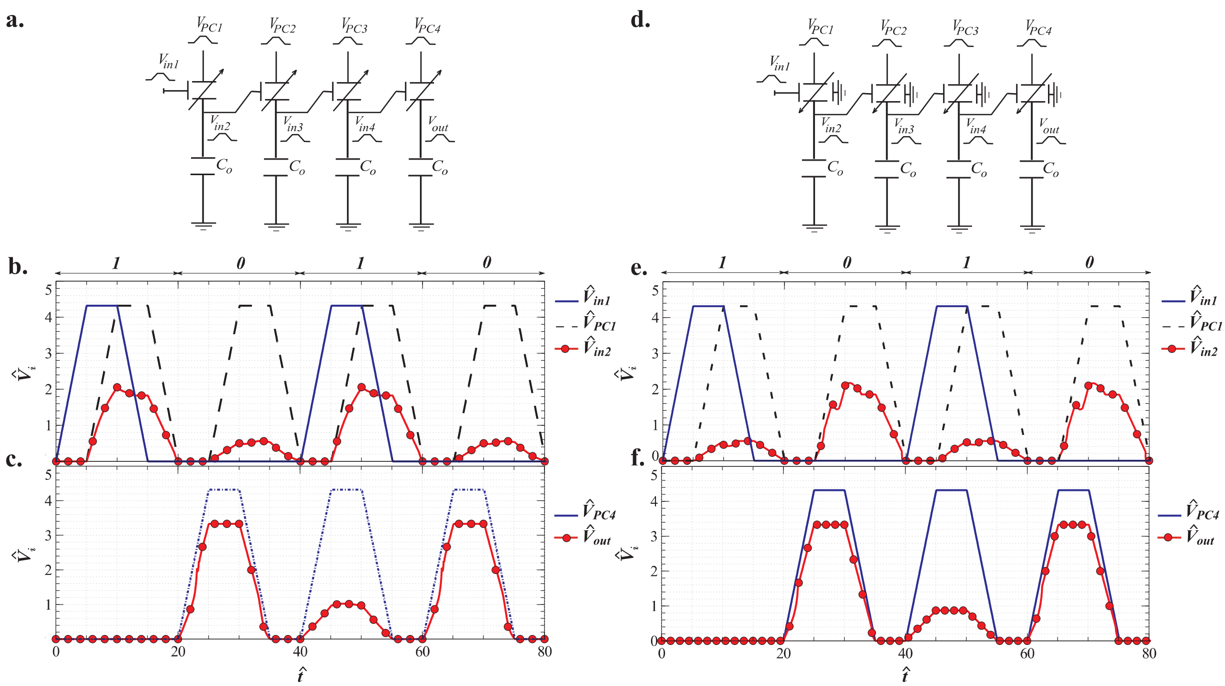

Fig. 7. Experiments of cascability. a, d) Tested circuits made of 4 cascaded buffers/inverters. b, c) Evolution of voltages in cascaded buffers. e, f) Evolution of voltages in cascaded inverters.

dissipated energy is equal to 0.9*fJ*. However, most of the input energy ($\hat{E}_{in} + \hat{E}_P$) is recovered: the ratio between the recovered and the input energy is 89%.

4.3. Cascability

Now we consider the circuit composed of four cascaded CAL buffers and inverters. The buffer and inverter chain circuits are presented in Fig. 7a,d respectively. Each gate is supplied by a PC, and the subsequent PCs are delayed by a quarter of period in order to satisfy the adiabatic conditions. The dynamic behavior of the cascaded buffers and inverters is given by the following non-dimensional equation:

$$\ddot{\hat{x}}_i + \lambda\dot{\hat{x}}_i + \hat{x}_i - \hat{V}_{in,i}{}^2\left[1+\frac{1}{(\beta_1 - \hat{x}_i)^2} + \frac{\gamma}{(\beta_2 + \hat{x})^{0.75}}\right] + \alpha\left(\alpha_1 \hat{V}_{DS,i}{}^2\left[\frac{1+\beta_4(\beta_5 + \hat{x}_i)}{(\beta_5 + \hat{x}_i)^2}\right] - \alpha_2 \hat{V}_{PC,i}{}^2\left[\frac{1+\beta_4(\beta_3 - \hat{x}_i)}{(\beta_3 - \hat{x}_i)^2}\right]\right) \tag{21}$$

where i refers to the position of the gate in the chain, ($\alpha_1 = -1$ and $\alpha_2 = 0$, for PVC configuration and $\alpha_1 = \alpha_2 = 1$ for NVC) and:

$$\hat{V}_{in,i\geq 2} = \frac{\hat{V}_{PC,i-1}C_{DS,i-1}}{C_{DS,i-1} + C_{g,i} + C_o}, \tag{22}$$

$$\hat{V}_{DS,i} = \hat{V}_{PC,i}(C_{g,i+1} + C_o)/(C_{DS,i} + C_{g,i+1} + C_o). \tag{23}$$

We studied the dynamical response of the cascaded elements to an input logic sequence V_{in1} (1010). Fig. 7b,e depict the dynamic output of the first gate for the buffer and inverter series. The logic state at the 4th gate for the buffer and inverter series are shown in Fig. 7c,f respectively. The high (1) level corresponds to 77% of the PC's maximum voltage (equal to 1.38 V) for both buffers and inverters chains, and the low (0) level corresponds to 23% and 20% of the PC for the buffers and the inverters chains respectively.

5. Conclusion

We have presented novel four-terminal variable capacitors (FTVC) based on silicon nano/micro technologies that can be used in Capacitive Adiabatic Logic. The FTVC intends to replace the field effect transistor (FET) in adiabatic logic in order to drastically reduce the energy consumption by avoiding the static losses and the non-adiabatic dissipation in classical CMOS circuits. It is a better alternative than nanorelays, also envisaged in adiabatic logic using electromechanical devices, because of the absence of resistive contact.

The electromechanical simulations demonstrated that with only two types of FTVC, it is possible to implement basic adiabatic logic functions as inverters and buffers. We also demonstrated for the first time the cascability of both class of devices. During one cycle, a buffer gate of $10 \times 2.5\,\mu m^2$, dissipated 0.9 *fJ*, which is in the same order of the energy dissipated by nano-scale FET transistors. However, it scales in the cube of the size. Gaining one order of magnitude in volume will allow to beat the dissipation of the state of the art of CMOS circuits: the simulations shows that a buffer gate of $1 \times 0.25\,\mu m^2$ would dissipate 0.7 aJ.

The simulations presented in this paper are performed with dimensions of devices that can be fabricated with classical MEMS and IC technologies. The characteristic dimension is 40 nm for both structures and gaps, and is still possible to achieve using photolithography as in last generations of IC technologies. In addition, there is much less steps in the fabrication process that for ICs and it does not require any expensive material. Reducing even more the dimensions will need the use of e-beam lithography, which is currently still quite expensive because of the longer time required for this step. Etching gaps in silicon at the nanometer scale would be also a challenge. However, reducing the size of the etching areas is very favorable to Deep Reactive Ion Etching of silicon because of an increase of the etching aspect-ratio (AR) with small dimensions: for instance in [29], Parasuraman et al have performed an AR of 125 for a gap of 35 nm.

When adiabatic conditions are satisfied, most of the provided energy (89%) is recovered after one cycle. This is a bit less than the non-contact device we have presented in [19]. However, the logic state differentiation has been dramatically improved from a few percents to more than 50%. This is a considerable advantage for a practical implementation.

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Appendix A. Supporting information

Supplementary data associated with this article can be found in the online version at doi:10.1016/j.nanoen.2018.10.059

References

[1] S. Houri, G. Billiot, M. Belleville, A. Valentian, H. Fanet, Limits of CMOS technology and interest of NEMS relays for adiabatic logic applications, IEEE TCAS 62 (2015) 1546–1554.
[2] A.P. Chandrakasan, S. Sheng, R.W. Brodersen, Low power CMOS digital design, IEEE J. Solid-State Circuits 27 (1992) 473–484.
[3] A. Bellaouar, M. Elmarsry, Low power digital VLSI design, Circuits Syst. (1995).
[4] K. Roy, S. Prasad, Low-Power CMOS VLSI Circuit Design, Wiley, 2000.
[5] E. Pop, Energy dissipation and transport in nanoscale devices, Nano Res. 3 (2010) 147–169.
[6] P. Teichmann, Adiabatic logic: future trend and system level perspective, Springe. Sci. Adv. Microelectron. (2012).
[7] R. Landauer, Irreversibility and heat generation in the computing process, IBM J. Res. Dev. 5 (1961) 183–191.
[8] M. Madami, D. Chiuchiù, G. Carlotti, L. Gammaitoni, Fundamental energy limits in the physics of nanomagnetic binary switches, Nano Energy 15 (2015) 313–320.
[9] H. Fanet, Ultra low power electronics and adiabatic solutions, Electron. Eng. Ser. ISTE (2016), https://doi.org/10.1002/9781119006541.
[10] Y. Moon, D.K. Jeong, An efficient charge recovery logic circuit, IEEE J. Solid State Circuits 31 (1996) 514–522.
[11] S. Paul, A.M. Schlaffer, J.A. Nossek, Optimal charging of capacitors, IEEE Trans. Circuits Syst. I: Fundam. Theory Appl. 47 (2000) 1009–1016.
[12] O.Y. Loh, H.D. Espinosa, Nanoelectromechanical contact switches, Nat. Nanotechnol. 7 (2012) 283–295.
[13] Z. Yi, J. Guo, Y. Chen, H. Zhang, S. Zhang, G. Xu, M. Yu, P. Cui, Vertical, capacitive microelectromechanical switches produced via direct writing of copper wires, Microsyst. Nanoeng. 2 (2016) 16010, https://doi.org/10.1038/micronano.2016.10.
[14] H. Kam, T.-J. King Liu, V. Stojanovic, D. Markovic, E. Alon, Design optimization and scaling of MEM relays for ultra-low power digital logic, IEEE Trans. Electron Devices 58 (2011) 236–250.
[15] C. Pawashe, K. Lin, K.J. Kuhn, Scaling limits of electrostatic nanorelays, IEEE Trans. Electron Devices 60 (2013) 2936–2942.
[16] M. Spencer, F. Chen, C.C. Wang, R. Nathanael, H. Fariborzi, A. Gupta, H. Kam, V. Pott, J. Jeon, T.-J. King Liu, D. Markovic, E. Alon, V. Stojanovic, Demonstration of integrated micro-electromechanical relay circuits for VLSI applications, IEEE J. Solid-State Circuits 4 (2011) 308–320.
[17] S. Houri, C. Poulain, A. Valentian, H. Fanet, Performance limits of nanoelectromechanical switches (NEMS)-based adiabatic logic circuits, J. Low Power Electron 3 (2013) 368–384.
[18] G. Pillonnet, H. Fanet, S. Houri, Adiabatic capacitive logic: a paradigm for low power logic, in: Circuits and Systems (ISCAS) IEEE International Symposium on, Baltimore, MD, USA, 28-31 May 2017, 2017.
[19] A. Galisultanov, Y. Perrin, H. Samaali, H. Fanet, P. Basset, G. Pillonnet, Contactless four-terminal MEMS variable capacitor for capacitive adiabatic logic, IOP Smart Mater. Struct. 25 (8) (2018), https://doi.org/10.1088/1361-665X/aacac4.
[20] C.H. Bennett, Logical reversibility of computation, IBM J. Res. Dev. 17 (1973) 525–532.
[21] J.G. Koller, W.C. Athas, Adiabatic switching, low energey computting, and the physics of storing and erasing information, Physics and Computation, PhysComp '92., Workshop on, Dallas, TX, USA, USA, 2-4 Oct, 1992.
[22] N.P. Vander Meijs, J.T. Fokkema, VLSI circuit reconstruction from mask topology, Integr. VLSI J. 2 (1984) 85–119.
[23] S.D. Senturia, Microsystem design, Springer US edition, 2001. ⟨http://dx.doi.org/10.1007/b117574⟩.
[24] H.B. Palmer, Capacitance of a parallel-plate capacitor by the Schwartz–Christoffel transformation, Trans. Am. Inst. Electr. Eng. 56 (1937) 363–366.
[25] A. Tazzoli, M. Barbato, Study of the actuation speed, bounces occurrences, and contact reliability of ohmic RF-MEMS switches, Microelectron. Reliab. 50 (2010) 1604–1608.
[26] A. Peschot, C. Poulain, N. Bonifaci, O. Lesaint, Contact bounce phenomena in a MEMS switch, in: IEEE Proceedings of the 58th Holm Conference on Electrical Contacts (Holm), 2012.
[27] T.B. Jones, N.G. Nenadic, Electromechanics and MEMS, Cambridge University Pres, 2013.
[28] G.M. Rebeiz, RF MEMS: Theory, Design, and Technology, John Wiley & Sons, 2004.
[29] J. Parasuraman, A. Summanwar, F. Marty, P. Basset, D.E. Angelescu, C. Bunel, T. Bourouina, Very high aspect ratio deep reactive ion etching of sub-micrometer trenches in silicon, Microelectron. Eng. 113 (2014) 35–39.

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